

CROSS-REFERENCES TO RELATED APPLICATION

10 **BACKGROUND**

2. Related Art

25 **[0005]** For example, the defects include a void at a bonding

interface of the two wafers, an edge void in a thin layer of a final structure (i.e., SOI substrate), and a bonding error due to a low bonding strength in the bonding interface. These defects may adversely affect properties of semiconductor devices fabricated using the SOI substrate.

[0006] As a result, there is a need for a technology to suppress wafer edge voids, suppress voids between the bonding interfaces of wafers, and strengthen the bonding strength of the bonding interface during fabricating the SOI substrate.

SUMMARY

[0007] Embodiments of the present disclosure provide a method of fabricating a SOI substrate that may be capable of reducing voids formed at a bonding interface of wafers.

[0008] Embodiments of the present disclosure provide a method of fabricating a SOI substrate that may be capable of improving bonding strength of the bonding interface of the wafers.

[0009] According to an embodiment of the present disclosure, there may be provided a method of fabricating an SOI substrate. A stopper layer, a semiconductor layer, a buried insulating layer and a first bonding insulation layer including a Silicon Carbon Nitride (SiCN) material may be sequentially formed on a sacrificial wafer. A second bonding insulation layer including the SiCN material may be formed on a reference wafer. Si-OH bonds may be formed in the first bonding insulation layer and the second bonding insulation layer by an O₂

plasma treatment and scrubbing of the first bonding insulation layer and the second bonding insulation layer. The sacrificial wafer may be bonded to the reference wafer to form a bonding structure such that the first bonding insulation layer and the second bonding insulation layer face each other. The bonding structure may then be annealed.

[0010] According to an embodiment of the present disclosure, there may be provided a method of fabricating an SOI substrate. A stopper layer, a semiconductor layer, a buried insulating layer and a first bonding insulation layer may be sequentially formed on a sacrificial wafer to generate a first structure. A second bonding insulation layer may be formed on a reference wafer to generate a second structure. Si-OH bonds may be formed in the first bonding insulation layer and the second bonding insulation layer. The first structure and the second structure may be bonded to form a bonding structure such that the first bonding insulation layer is bonded to the second bonding insulation layer

[0011] According to embodiments of the present disclosure, by using the SiCN as a wafer bonding insulation layer, it may be possible to effectively adsorb an H₂ gas outgassing from the sacrificial wafer during high temperature annealing after bonding, thereby inhibiting formations of voids at the interface between the bonding insulation layers.

[0012] Further, the O₂ plasma treatment of the SiCN may break the Si-C bonds and may scrub to form the Si-OH bonds to induce van der Waals hydrogen bonds (Si-OH---OH-Si) between the bonding

insulation layers, by changing the van der Waals hydrogen bonds (Si-OH---OH-Si) into Si-O-Si covalent bonds through the annealing, the bonding may be strengthened by decreasing the bond length and decreasing an interfacial gap between the bonding insulation layers.

5 **[0013]** Furthermore, by bonding the sacrificial and reference wafers at a room temperature after a helium gas injection for a set period of time, the generation of wafer edge voids due to the Joule-Thomson effect may be prevented.

10 **BRIEF DESCRIPTION OF THE DRAWINGS**

[0014] The above and another aspects, features, and advantages of the embodiments of the present disclosure will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings, in which:

15 **[0015]** FIG. 1 is a flow chart illustrating a method of fabricating an SOI substrate in accordance with embodiments of the present disclosure; and

[0016] FIGS. 2 to 10 are cross-sectional views illustrating a method of fabricating SOI substrates in accordance with embodiments
20 of the present disclosure.

DETAILED DESCRIPTION

[0017] Various embodiments of the present disclosure will be described in greater detail with reference to the accompanying
25 drawings. The drawings are schematic illustrations of various

embodiments and intermediate structures. As such, variations from the configurations and shapes of the illustrations as a result, for example, of manufacturing techniques and/or tolerances, are to be expected. Thus, the described embodiments should not be construed
5 as being limited to the particular configurations and shapes illustrated herein but may include deviations in configurations and shapes which do not depart from the spirit and scope of the present disclosure as defined in the appended claims.

[0018] The embodiments of the present disclosure are described
10 herein with reference to cross-section and/or plan illustrations of the embodiments. However, embodiments of the present disclosure should not be construed as limiting the inventive concept. Although a few embodiments of the present disclosure will be shown and described, it will be appreciated by those of ordinary skill in the art that changes
15 may be made in these embodiments without departing from the principles and spirit of the present disclosure.

[0019] FIG. 1 is a flow chart illustrating a method of fabricating an SOI substrate in accordance with embodiments of the present disclosure. FIGS. 2 to 10 are cross-sectional views illustrating a method
20 of fabricating an SOI substrate in accordance with embodiments of the present disclosure.

[0020] Referring to FIGS. 1 and 2, a first treatment may be performed on a sacrificial wafer 110 (S10). For example, the first treatment may include a first cleaning process. The sacrificial wafer
25 110 may include at least one material selected from silicon (Si),

germanium (Ge), silicon carbide (SiC), IV-IV group, III-V group, or II-VI group semiconductor compounds, and piezoelectric materials (e.g., LiNbO₃, LiTaO₃, etc.).

[0021] In some embodiments, the first treatment may include
5 cleaning the sacrificial wafer 110 using a SC1 solution (NH₄OH:H₂O₂:H₂O). During the cleaning of the sacrificial wafer 110, an oxide layer 110a including impurities (or residues) on a surface of the sacrificial wafer 110 is removed. The surface of the sacrificial wafer 110 may include an upper surface, a bottom surface and sidewalls. For
10 example, the oxide layer 110a including the impurities may be formed on the surface of the sacrificial wafer 110 by H₂O₂ component of the SC1 solution. In some embodiments, the oxide layer 110a including the impurities may be removed by the NH₄OH component with a property of etching an oxide material in the SC1 solution. Thus, the
15 impurities existing on the surface of the sacrificial wafer 110 may be firstly removed.

[0022] The impurities remaining on the surface of the sacrificial wafer 110 may be removed by the oxide layer 110a generated by the first treatment. Referring to FIG. 1 and FIG. 3, a chemical oxide layer
20 110b generated as a by-product by H₂O₂ of the SC1 solution during the first treatment may remain despite the NH₄OH component of the SC1 solution.

[0023] The sacrificial wafer 110 may be performed by a H₂ bake process under a high temperature. (S20). Accordingly, the chemical
25 oxide layer 110b on the surface of the sacrificial wafer 110 may be

removed by the H₂ bake process. For example, impurities in a bevel region of the sacrificial wafer 110 may be effectively removed by the H₂ bake process. Thus, dislocation defects due to lattice mismatch may be reduced by removing the impurities in the bevel region of the sacrificial wafer 110.

[0024] Referring to FIGS. 1 and 4, a stopper layer 111 and a semiconductor layer 112 may be sequentially formed on the sacrificial wafer 110 using an epitaxial growth process (S30). In some embodiments, the stopper layer 111 and the semiconductor layer 112 may be formed by an in-situ process.

[0025] For example, the stopper layer 111 may prevent the semiconductor layer 112 from being removed, when the sacrificial wafer 110 may be removed from a bonding structure to be performed later. The stopper layer 111 may be formed using a material having a different etching selectivity from an etching selectivity of the sacrificial wafer 110 and the semiconductor layer 112. Further, the stopper layer 111 may be formed using a material with a small difference in properties from the semiconductor layer 112. In some embodiments, the stopper layer 111 may include a single crystalline silicon germanium (SiGe) layer, and the semiconductor layer 112 may include a single crystalline silicon (Si) layer.

[0026] Referring to FIGS. 1 and 5, a buried insulation layer 113 may be formed over the semiconductor layer 112 (S40). For example, the buried insulation layer 113 may include, but is not limited to, a silicon oxide (SiO₂) layer.

[0027] Referring to FIGS. 1, 6A and 6B, a first bonding insulation layer 114 may be formed over the sacrificial wafer 110. Further, a reference wafer 120 is prepared. A second bonding insulation layer 124 may be formed on the reference wafer 120 (S50). In some
5 embodiments, the first bonding insulation layer 114 may be formed to contact the buried insulation layer 113 over the sacrificial wafer 110. The second bonding insulation layer 124 may be formed on a surface of the reference wafer 120. The reference wafer 120 may include at least one material selected from Si, Ge, SiC, IV-IV group, III-V group,
10 or II-VI group semiconductor compounds, and piezoelectric materials (e.g., LiNbO₃, LiTaO₃, etc.).

[0028] For example, forming the first bonding insulation layer 114 on the buried insulation layer 113 and forming the second bonding insulation layer 124 on the reference wafer 120 may be performed
15 alternately in a same chamber, or may be performed simultaneously in a same chamber, or may be performed simultaneously in different chambers.

[0029] In some embodiments, the first bonding insulation layer 114 and the second bonding insulation layer 124 may include a silicon
20 carbon nitride (SiCN) layer. For example, the first bonding insulation layer 114 and the second bonding insulation layer 124 may be formed by a plasma-enhanced chemical vapor deposition (PECVD) process, respectively. When the first bonding insulation layer 114 and the second bonding insulation layer 124 are formed in a PECVD chamber,
25 tetramethylsilane (TMS) gas, nitrogen (N₂) gas, and helium (He) gas

are provided to the PECVD chamber, to stabilize the first bonding insulation layer 114 as a plasma treatment.

[0030] By way of example and without any limitation, a carbon (C) concentration ratio of each of the first and second bonding insulation layers 114 and 124 may be greater than about 36%. As the
5 carbon (C) concentration ratio of each of the first and second bonding insulating layers 114 and 124 increases, the number of Si dangling bonds generated in each of the first and second bonding insulating layers 114 and 124 during a subsequent Oxygen (O₂) plasma
10 treatment may also increase. Thus, the H₂ gas generated and remaining in the H₂ bake process and outgassed may be more effectively adsorbed to suppress voids.

[0031] Referring to FIGS. 1, 7A and 7B, the O₂ plasma treatment may be performed on the first bonding insulation layer 114 and the
15 second bonding insulation layer 124 (S60). For example, an O₂ gas may be injected into a process chamber, for example, a plasma chamber. Then, the process chamber is stabilized for a period of time, for example, about 30 seconds. Thereafter, a HF power of 50W to 400W may be applied to the process chamber for a set time period, for
20 example, 10 seconds, and then the first bonding insulation layer 114 and the second bonding insulation layer 124 may be performed by the O₂ plasma treatment respectively

[0032] Si-C bonds of each of the first and second bonding insulation layers 114 and 124 which include the SiCN material are
25 desorbed from carbon (C) by the O₂ plasma treatment. Accordingly,

first and second bonding insulation layers 114D and 124D have a higher content of silicon dangling bonds than the SiCN material before the O₂ plasma treatment.

[0033] Referring to FIGS. 1, 8A and 8B, the sacrificial wafer 110 and the reference wafer 120 may be scrubbed to remove particles (S70). For example, the particles resulting from previous processes may be generated on surfaces of the sacrificial wafer 110 and the reference wafer 120 after the O₂ plasma treatment. The scrubbing process (S70) of the sacrificial wafer 110 and the reference wafer 120 may include a rinse process and a drying process. For example, the rinse process may be performed by a deionized water (DIW). The drying process may be performed by an N₂ dryer for a period of time (e.g., about 30 seconds). For example, the scrubbing process may be performed in a scrubber.

[0034] As OH bonds of the H₂O provided by the DIW are adsorbed on the Si dangling bonds of the first and second bonding insulation layers 114D and 124D in FIGS. 7A and 7B, first and second bonding insulation layers 114H and 124H having Si-OH bonds may be formed, as shown in FIGS. 8A and 8B.

[0035] Referring to FIGS. 1 and 9, a structure of the sacrificial wafer 110, the stopper layer 111, the semiconductor layer 112, the buried insulation layer 113 and the first bonding insulation layer 114H may be flipped over. The flipped structure may be bonded onto a structure of the reference wafer 120 and the second bonding insulation layer 124H (S80).

[0036] For example, the sacrificial wafer 110 may be chucked face-down on the upper chuck (not shown) of a bonding apparatus (not shown) and the reference wafer 120 may be chucked on the lower chuck (not shown) of the bonding apparatus. In this embodiment, the sacrificial wafer 110 and the reference wafer 120 may be chucked onto the upper chuck and the lower chuck in a vacuum adsorption manner.

[0037] In some embodiments, a helium gas may be injected into the process chamber for a set time period (e.g., about 35 seconds or more) while the sacrificial wafer 110 and the reference wafer 120 may be chucked on the upper chuck and the lower chuck, respectively. After the set time period, the vacuum in the upper chuck on which the sacrificial wafer 110 may be chucked may be released, allowing the sacrificial wafer 110 to detach from the upper chuck and fall onto the reference wafer 120 for bonding.

[0038] As such, by injecting the helium gas with a negative Joule-Thomson coefficient for a set period of time prior to bonding the sacrificial wafer 110 and the reference wafer 120, generations of edge voids due to a Joule-Thomson effect may be suppressed.

[0039] Further, as the sacrificial wafer 110 and the reference wafer 120 may be bonded to each other such that the first and second bonding insulation layers 114H and 124H having Si-OH bonds contact each other, as described above, the first bonding insulation layer 114H and the second bonding insulation layer 124H may be bonded by van der Waals hydrogen bonds (Si-OH---OH-Si) between the Si-OH bonds of the first bonding insulation layer 114H and the Si-OH bonds of the

second bonding insulation layer 124H on the reference wafer 120. As a result, a bonding structure including the second bonding insulation layer 124H and the first bonding insulation layer 114H bonded by the van der Waals hydrogen bonds (Si-OH---OH-Si), the buried insulating layer 113, the semiconductor layer 112, the stopper layer 111, and the sacrificial wafer 110 arranged sequentially on the reference wafer 120 may be formed.

[0040] Referring to FIGS. 1 and 10, the bonding structure may be processed by an annealing process (S90). By way of example and without any limitation, the annealing process may be performed at about 430°C. In some embodiments, as the annealing process is performed at a high temperature, H₂O may escape from a van der Waals hydrogen bond (Si-OH---OH-Si) between the first bonding insulation layer 114H and the second bonding insulation layer 124H to form a Si-O-Si covalent bond, thereby reducing a length of the bond. Accordingly, an interfacial gap between the first and second bonding insulation layers 114B and 124B may be reduced, thereby enhancing the bond strength, as shown in FIG. 10.

[0041] As described in S20 of FIG. 1, a H₂ thermal treatment at a high temperature may be performed to remove the chemical oxide layer 110b on the surface of the sacrificial wafer 110. In this operation, the H₂ gas may be stored in the sacrificial wafer 110 at the same time as the chemical oxide layer 110b may be removed. There may be a concern that the H₂ gas stored in the sacrificial wafer 110 may be outgassed to a bonding interface (e.g., a portion of the bonding surface

between the first bonding insulation layer and the second bonding insulation layer) having a relatively weak bonding strength during the high temperature annealing, resulting in the formation of voids. However, in some embodiments, the outgassed H_2 may be effectively
5 adsorbed on N bonds of the SiCN material used as the bonding insulation layers 114B and 124B, thereby preventing the formation of a void at the bonding interface between the bonding insulation layers 114B and 124B.

[0042] As described above, in some embodiments, the bonding
10 insulation layer may be formed with the SiCN over each of the sacrificial wafer 110 and the reference wafer 120, the O_2 plasma treatment may be performed on the SiCN to form the Si dangling bond, and the OH may be adsorbed on the Si dangling bond during the scrubbing process to form the bonding insulation layer having Si-OH bonds. The bonding
15 insulation layers having Si-OH bonds may be bonded by van der Waals hydrogen bonds ($Si-OH---OH-Si$), and upon the annealing process, the Si-O-Si covalent bonds may be formed as the H_2O escapes from the van der Waals hydrogen bonds ($Si-OH---OH-Si$). As such, the interfacial gap between the bonding insulation layers may be reduced
20 as the bond length decreases, thereby strengthening the bonding between the bonding insulation layers. In some embodiments and without any limitation, the bonding strength between the bonding insulation layers after completion of annealing process may be $1.8 J/m^2$ or more.

25 **[0043]** In some embodiments, once the annealing process of the

bonding structure may be complete, the sacrificial wafer 110 and stopper layer 111 may be sequentially removed to complete fabrication of the SOI substrate.

[0044] For example, the sacrificial wafer 110 disposed on the bonding structure may have a part of an edge removed through a wafer trimming before the bonding process of the sacrificial wafer 110 and the reference wafer 120. Then, the sacrificial wafer 110 may be removed through a grinding process after the bonding and annealing processes so that the sacrificial wafer 110 has a set thickness (or height). Thereafter, a remaining sacrificial wafer and the stopper layer 111 may be sequentially removed.

[0045] The remaining sacrificial wafers may be removed using a wet cleaning process and a dry cleaning process. For example, the remaining sacrificial wafer may be removed by successively performing a Dilute hydrofluoric acid (DHF) pretreatment cleaning process and a wet alkaline (Diluted NH_4OH , TMAH: $(\text{CH}_3)_4\text{N}(\text{OH})$, KOH, etc.) post-treatment cleaning process, followed by the drying process in an IPA Dryer. Furthermore, the stopper layer 111 may be removed using the wet cleaning process and the dry cleaning process. For example, the stopper layer 111 may be removed by a wet alkaline (Diluted NH_4OH , TMAH: $(\text{CH}_3)_4\text{N}(\text{OH})$, KOH, etc.) cleaning process and a dry cleaning process using fluorinated compounds.

[0046] As described above, by sequentially removing the remaining sacrificial wafer and stopper layer 111, fabrication of the SOI substrate including the reference wafer 120 and the second bonding

insulation layer 124, the first bonding insulation layer 114, the buried insulating layer 113, and the semiconductor layer 112 sequentially stacked on the reference wafer 120 may be completed.

[0047] The above described embodiments of the present disclosure are intended to illustrate and not to limit the present invention. Various alternatives and equivalents are possible. The embodiments of the present disclosure are not limited by the embodiments described herein. Nor are the embodiments limited to any specific type of semiconductor device. Other additions, subtractions, or modifications are possible in view of the present disclosure and are intended to fall within the scope of the appended claims. Furthermore, the embodiments may be combined to form additional embodiments.

WHAT IS CLAIMED IS:

1. A method of fabricating a silicon on insulator (SOI) substrate, the method comprising:

5 sequentially forming, on a sacrificial wafer, a stopper layer, a semiconductor layer, a buried insulating layer and a first bonding insulation layer including a Silicon Carbon Nitride (SiCN) material;

forming a second bonding insulation layer including the SiCN material on a reference wafer;

10 forming Si-OH bonds in the first bonding insulation layer and the second bonding insulation layer, by performing an O₂ plasma treatment and scrubbing of the first bonding insulation layer and the second bonding insulation layer, respectively;

15 bonding the sacrificial wafer and the reference wafer to form a bonding structure such that the first bonding insulation layer and the second bonding insulation layer face each other; and

annealing the bonding structure.

2. The method of claim 1, further comprising:

20 cleaning the sacrificial wafer before forming the stopping layer on the sacrificial wafer.

3. The method of claim 2,
wherein cleaning the sacrificial wafer comprises:

25 cleaning the sacrificial wafer using a SC1 solution

($\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$), wherein an oxide layer including impurities is formed on a surface of the sacrificial wafer, and then removed during the cleaning of the sacrificial wafer; and

removing a chemical oxide layer formed on the sacrificial wafer
5 by a H_2 bake treatment at high temperature on the sacrificial wafer.

4. The method of claim 1,
wherein at least one of the stopper layer and the semiconductor
layer is formed by an epitaxial growth process on the sacrificial wafer.

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5. The method of claim 1,
wherein the stopper layer comprises single crystalline silicon
germanium (SiGe), and

wherein the semiconductor layer comprises single crystalline
15 silicon (Si).

6. The method of claim 1,
wherein forming the Si-OH bonds in the first bonding insulation
layer and the second bonding insulation layer comprises:

20 changing Si-C bonds of the first bonding insulation layer and the
second bonding insulation layer into Si dangling bonds by performing
the O_2 plasma treatment; and

adsorbing OH bonds onto the Si dangling bond using H_2O
provided by the scrubbing.

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7. The method of claim 1,
wherein forming the bonding structure comprises:
flipping the sacrificial wafer over and chucking the sacrificial
wafer into an upper chuck of a bonding apparatus;
5 chucking the reference wafer into a lower chuck of the bonding
apparatus;
injecting a He gas into the bonding apparatus; and
dechucking the sacrificial wafer from the upper chuck so that the
sacrificial wafer is bonded to the reference wafer.

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8. The method of claim 1,
wherein the O₂ plasma treatment comprises:
injecting an O₂ gas into a process chamber;
stabilizing the process chamber; and
15 applying HF power to the O₂ gas.

9. The method of claim 1,
wherein at least one of the first and second bonding insulation
layers include a SiCN layer formed through a plasma-enhanced
20 chemical vapor deposition (PECVD) process, and
wherein each of the first and second bonding insulation layers is
formed through a plasma treatment after stabilization by injecting a
tetramethylsilane (TMS) gas, a nitrogen gas and a helium gas.

25 10. The method of claim 1,

wherein a carbon (C) concentration ratio of the SiCN material is no less than 36%.

11. The method of claim 1, further comprising:
5 sequentially removing the sacrificial wafer and the stopper layer from the bonding structure after annealing the bonding structure.

12. The method of claim 11,
wherein the sacrificial wafer and the stopper layer are removed
10 using a wet cleaning process and a dry cleaning process, respectively.

13. A method of fabricating a silicon on insulator (SOI) substrate, the method comprising:
sequentially forming, on a sacrificial wafer, a stopper layer, a
15 semiconductor layer, a buried insulating layer and a first bonding insulation layer to generate a first structure;
forming a second bonding insulation layer on a reference wafer to generate a second structure;
forming Si-OH bonds in the first bonding insulation layer and the
20 second bonding insulation layer; and
bonding the first structure and the second structure to form a bonding structure such that the first bonding insulation layer is bonded to the second bonding insulation layer.

25 14. The method of claim 13, further comprising:

annealing the bonding structure.