

**IMAGE COMPRESSION COPROCESSOR WITH DATA FLOW
CONTROL AND MULTIPLE PROCESSING UNITS**

Abstract

The present invention provides an image compression/decompression (410) which is integrated on a single chip. The control bus has a control unit (418) which is connected by an internal, global bus (416) to a number of different, special purpose processing units (414, 420, 422, 426 and 428). Each of the processing units is specifically designed to handle only certain steps in compression and decompression processes.

[Figure 2]

