CLAIMS

WHAT IS CLAIMED:

1. A method, comprising:

performing a plurality of material deposition cycles to form a high-k dielectric layer above a semiconductor material layer; and

introducing a passivating material into a gaseous precursor that is used for forming said high-k dielectric layer during at least one of said plurality of material deposition cycles.

2. The method of claim 1, wherein each of said plurality of material deposition cycles is a self-limiting deposition cycle of an atomic layer deposition process.

3. The method of claim 1, further comprising forming an interfacial layer above said semiconductor material layer and forming said high-k dielectric layer above said interfacial layer.

4. The method of claim 3, further comprising exposing a surface of said interfacial layer to a gaseous treatment ambient prior to performing an initial one of said plurality of material deposition cycles, said gaseous treatment ambient comprising said passivating material.

5. The method of claim 1, wherein said passivating material comprises one of fluorine and chlorine.

6. A method, comprising:

forming a layer of high-k dielectric material above a semiconductor layer of a semiconductor device by performing an atomic layer deposition process comprising a plurality of self-limiting deposition cycles, wherein performing each of said plurality of self-limiting deposition cycles comprises forming a sub-layer of said layer of high-k dielectric material by exposing said semiconductor device to a deposition ambient comprising a flow of a first gaseous precursor, said first gaseous precursor comprising a material component of said layer of high-k dielectric material; and

modifying said deposition ambient during at least one of said plurality of self-limiting deposition cycles to comprise a flow of a second gaseous precursor, said second gaseous precursor comprising a passivating material.

7. The method of claim 6, further comprising, during said atomic layer deposition process, interrupting said flow of said first gaseous precursor and exposing a surface of at least one of said sub-layers of said layer of high-k dielectric material to a gaseous treatment ambient comprising said second gaseous precursor.

8. The method of claim 6, further comprising modifying said deposition ambient during an initial one of said plurality of self-limiting deposition cycles.

9. The method of claim 6, further comprising modifying said deposition ambient after performing an initial one of said plurality of self-limiting deposition cycles.

10. The method of claim 6, further comprising alternatingly forming first and second sub-layer groups, wherein each of said first and second sub-layer groups comprises at least one sub-layer, wherein each sub-layer of said first sub-layer group is formed using said modified deposition ambient, and wherein each sub-layer of said second sub-layer group is formed without using said modified deposition ambient.

11. The method of claim 6, further comprising forming an interfacial layer above said semiconductor layer and forming said layer of high-k dielectric material above said interfacial layer.

12. The method of claim 11, further comprising exposing a surface of said interfacial layer to a gaseous treatment ambient prior to forming said layer of high-k dielectric material, said gaseous treatment ambient comprising said second gaseous precursor.

13. The method of claim 6, wherein said high-k dielectric material comprises hafnium dioxide and said first gaseous precursor comprises hafnium tetrachloride.

14. The method of claim 6, wherein said passivating material comprises one of fluorine and chlorine.

15. The method of claim 6, wherein said passivating material comprises fluorine and said second gaseous precursor comprises one of nitrogen trifluoride and hydrogen tetrafluoride.

16. The method of claim 6, further comprising controlling an amount of said passivating material that is incorporated into said layer of high-k dielectric material by adjusting at least one process parameter of said modified deposition ambient that is used to perform said at least one of said plurality of self-limiting deposition cycles.

17. The method of claim 16, wherein adjusting said at least one process parameter of said modified deposition ambient comprises adjusting at least one of a reaction temperature, chamber pressure, flow rate of said first gaseous precursor, and flow rate of said second gaseous precursor.

18. A method, comprising:

forming an interfacial layer above a semiconductor layer of a semiconductor device;

performing an atomic layer deposition process to deposit a high-k dielectric layer above said interfacial layer, wherein performing said atomic layer deposition process comprises exposing said semiconductor device to a first gaseous precursor;

incorporating a passivating material into said high-k dielectric layer, wherein incorporating said passivating material comprises combining a second gaseous precursor with said first gaseous precursor during at least one deposition cycle of said atomic layer deposition process; and

controlling an amount of said passivating material that is incorporated into said high-k dielectric layer, wherein controlling said amount comprises adjusting at least one of a reaction temperature, chamber pressure, flow rate of said first gaseous precursor, and flow rate of said second gaseous precursor during said at least one deposition cycle.

19. The method of claim 18, wherein said high-k dielectric layer comprises hafnium dioxide and said first gaseous precursor comprises hafnium tetrachloride.

20. The method of claim 18, wherein said passivating material comprises fluorine and said second gaseous precursor comprises one of nitrogen trifluoride and hydrogen tetrachloride.

21. The method of claim 18, further comprising forming a metal gate electrode material layer above said high-k dielectric layer.

CLAIMS

1. A method, comprising:

performing a plurality of material deposition cycles to form a high-k dielectric layer above a semiconductor material layer; and

introducing a passivating material into a gaseous precursor that is used for forming said high-k dielectric layer during at least one of said plurality of material deposition cycles.

2. The method of claim 1, further comprising forming an interfacial layer above said semiconductor material layer and forming said high-k dielectric layer above said interfacial layer.

3. The method of claim 2, further comprising exposing a surface of said interfacial layer to a gaseous treatment ambient prior to performing an initial one of said plurality of material deposition cycles, said gaseous treatment ambient comprising said passivating material.

4. The method of claim 1, wherein said passivating material comprises one of fluorine and chlorine.

5. A method, comprising:

forming a layer of high-k dielectric material above a semiconductor layer of a semiconductor device by performing an atomic layer deposition process comprising a plurality of self-limiting deposition cycles, wherein performing each of said plurality of self-limiting deposition cycles comprises forming a sub-layer of said layer of high-k dielectric material by exposing said semiconductor device to a deposition ambient comprising a flow of a first gaseous precursor, said first gaseous precursor comprising a material component of said layer of high-k dielectric material; and

modifying said deposition ambient during at least one of said plurality of self-limiting deposition cycles to comprise a flow of a second gaseous precursor, said second gaseous precursor comprising a passivating material.

6. The method of claim 5, further comprising, during said atomic layer deposition process, interrupting said flow of said first gaseous precursor and exposing a surface of at least one of said sub-layers of said layer of high-k dielectric material to a gaseous treatment ambient comprising said second gaseous precursor.

7. The method of claim 5, further comprising modifying said deposition ambient during an initial one of said plurality of self-limiting deposition cycles.

8. The method of claim 5, further comprising modifying said deposition ambient after performing an initial one of said plurality of self-limiting deposition cycles.

9. The method of claim 5, further comprising alternatingly forming first and second sub-layer groups, wherein each of said first and second sub-layer groups comprises at least one sub-layer, wherein each sub-layer of said first sub-layer group is formed using said modified deposition ambient, and wherein each sub-layer of said second sub-layer group is formed without using said modified deposition ambient.

10. The method of claim 5, further comprising forming an interfacial layer above said semiconductor layer and forming said layer of high-k dielectric material above said interfacial layer.

11. The method of claim 10, further comprising exposing a surface of said interfacial layer to a gaseous treatment ambient prior to forming said layer of high-k dielectric material, said gaseous treatment ambient comprising said second gaseous precursor.

12. The method of claim 5, wherein said high-k dielectric material comprises hafnium dioxide and said first gaseous precursor comprises hafnium tetrachloride.

13. The method of claim 5, wherein said passivating material comprises one of fluorine and chlorine.

14. The method of claim 5, wherein said passivating material comprises fluorine and said second gaseous precursor comprises one of nitrogen trifluoride and hydrogen tetrafluoride.

15. The method of claim 5, wherein modifying said deposition ambient during said at least one of said plurality of self-limiting deposition cycles comprises controlling an amount of said passivating material that is incorporated into said layer of high-k dielectric material by adjusting at least one process parameter of said modified deposition ambient.

16. The method of claim 15, wherein adjusting said at least one process parameter of said modified deposition ambient comprises adjusting at least one of a reaction temperature, chamber pressure, flow rate of said first gaseous precursor, and flow rate of said second gaseous precursor.

17. A method, comprising:

forming an interfacial layer above a semiconductor layer of a semiconductor device;

performing an atomic layer deposition process to deposit a high-k dielectric layer above said interfacial layer, wherein performing said atomic layer deposition process comprises exposing said semiconductor device to a first gaseous precursor;

incorporating a passivating material into said high-k dielectric layer, wherein incorporating said passivating material comprises combining a second gaseous precursor with said first gaseous precursor during at least one deposition cycle of said atomic layer deposition process; and

controlling an amount of said passivating material that is incorporated into said high-k dielectric layer, wherein controlling said amount comprises adjusting at least one of a reaction temperature, chamber pressure, flow rate of said first gaseous precursor, and flow rate of said second gaseous precursor during said at least one deposition cycle.

18. The method of claim 17, wherein said high-k dielectric layer comprises hafnium dioxide and said first gaseous precursor comprises hafnium tetrachloride.

19. The method of claim 17, wherein said passivating material comprises fluorine and said second gaseous precursor comprises one of nitrogen trifluoride and hydrogen tetrachloride.

20. The method of claim 17, further comprising forming a metal gate electrode material layer above said high-k dielectric layer.

21. The method of claim 1, wherein performing each of said plurality of material deposition cycles comprises performing a plurality of sequential pulse/purge steps.

22. The method of claim 21, wherein performing said plurality of sequential pulse/purge steps comprises:

performing a first pulse step in a reaction chamber to expose a surface where said high-k dielectric layer is being formed to said gaseous precursor, wherein a first material sub-layer is formed above said surface during said first pulse step;

after performing said first pulse step, performing a first purge step to remove at least reaction by products from said reaction chamber;

after performing said first purge step, performing a second pulse to introduce an oxidant into said reaction chamber; and

after performing said second pulse step, performing a second purge step to remove said oxidant from said reaction chamber.

23. A semiconductor device comprising a semiconductor material layer, formed by a method in accordance with any one of the claims 1 to 16.

24. A semiconductor device comprising a semiconductor layer, formed by a method in accordance with any one of the claims 17 to 22.