

WHAT IS CLAIMED IS:

1. A semiconductor processing chamber, comprising:
a showerhead;
a pedestal configured to support a semiconductor substrate, wherein the
5 showerhead and pedestal at least partially define a processing region within the semiconductor
processing chamber;
a spacer characterized by a first surface in contact with the showerhead and a
second surface opposite the first surface; and
a pumping liner characterized by a first surface in contact with the spacer, and a
10 second surface opposite the first surface, wherein the pumping liner defines a plurality of
apertures within the first surface of the pumping liner.
2. The semiconductor processing chamber of claim 1, wherein the spacer
comprises an annulus, and wherein an inner annular sidewall of the spacer extending between the
first surface of the spacer and the second surface of the spacer at least partially defines the
15 processing region.
3. The semiconductor processing chamber of claim 2, wherein the inner
annular sidewall of the spacer is at least partially characterized by an arcuate profile extending
away from the processing region in a direction towards the second surface of the spacer.
4. The semiconductor processing chamber of claim 3, wherein the inner
20 annular sidewall of the spacer at the second surface of the spacer is positioned radially outward
of the plurality of apertures within the first surface of the pumping liner.
5. The semiconductor processing chamber of claim 1, wherein the second
surface of the spacer is seated on the pumping liner.
6. The semiconductor processing chamber of claim 1, wherein the pumping
25 liner comprises an annulus characterized by an inner annular sidewall and an outer annular
sidewall, and wherein the pumping liner defines a plenum between the inner annular sidewall
and the outer annular sidewall.

7. The semiconductor processing chamber of claim 6, wherein the plurality of apertures provide fluid access to the plenum from the first surface of the pumping liner.

8. The semiconductor processing chamber of claim 6, wherein the inner annular sidewall of the pumping liner extends vertically to define a rim protruding from the first surface of the pumping liner at the inner annular sidewall.

9. The semiconductor processing chamber of claim 8, wherein the pedestal is vertically translatable within the processing region of the semiconductor processing chamber, and wherein the pedestal comprises a platen and a stem extending from a backside of the platen.

10. The semiconductor processing chamber of claim 9, wherein, when the pedestal is in a raised operational position proximate the showerhead, a plane across the backside of the platen is maintained below an upper surface of the rim protruding from the first surface of the pumping liner.

11. A semiconductor processing chamber pumping liner, comprising:
an annular member characterized by:
a first surface, wherein a plurality of apertures are defined through the first surface of the annular member,
a second surface opposite the first surface,
an inner annular sidewall, and
an outer annular sidewall.

12. The semiconductor processing chamber pumping liner of claim 11, wherein the second surface defines a plenum about the annular member extending towards the first surface between the inner annular sidewall and the outer annular sidewall.

13. The semiconductor processing chamber pumping liner of claim 12, wherein the plurality of apertures provide fluid access to the plenum through the first surface of the annular member.

14. The semiconductor processing chamber pumping liner of claim 11, wherein the inner annular sidewall of the annular member extends vertically to define a rim protruding from the first surface at the inner annular sidewall.

15. The semiconductor processing chamber pumping liner of claim 14,
5 wherein the rim extends continuously about the inner annular sidewall.

16. A method of semiconductor processing, the method comprising:
flowing an etchant precursor into a remote plasma region of a semiconductor
processing chamber;
generating plasma effluents of the etchant precursor within the remote plasma
10 region of the semiconductor processing chamber;
flowing the plasma effluents of the etchant precursor through a showerhead into a
processing region of the semiconductor processing chamber;
contacting a substrate with the plasma effluents, wherein the substrate is seated on
a pedestal; and
15 exhausting etch byproducts from the processing region through a pumping liner
characterized by a first surface facing the showerhead and a second surface opposite the first
surface, wherein the pumping liner defines a plurality of apertures within the first surface of the
pumping liner.

17. The method of semiconductor processing of claim 16, wherein the
20 semiconductor processing chamber further comprises a spacer characterized by a first surface in
contact with the showerhead and a second surface opposite the first surface and in contact with
the pumping liner, wherein the spacer comprises an annulus, and wherein an inner annular
sidewall of the spacer extending between the first surface of the spacer and the second surface of
the spacer at least partially defines the processing region.

18. The method of semiconductor processing of claim 17, wherein the inner
25 annular sidewall of the spacer is at least partially characterized by an arcuate profile extending
away from the processing region in a direction towards the second surface of the spacer.

19. The method of semiconductor processing of claim 18, wherein the inner annular sidewall of the spacer at the second surface of the spacer is positioned radially outward of the plurality of apertures within the first surface of the pumping liner.

20. The method of semiconductor processing of claim 16, wherein the
5 pumping liner is further characterized by an inner annular sidewall, and wherein the inner annular sidewall extends vertically to define a rim protruding from the first surface of the pumping liner at the inner annular sidewall.