

METHOD FOR IN-LINE OPTICAL TESTING

Field of the Invention

The present invention relates to the field of photonics and more particularly to a method for in-line optical testing.

5 Background of the Invention

In integrated photonics fabrication, optical waveguide layers are typically formed in initial stages of fabrication and are subsequently covered with dielectric cladding and metal layers. Efficient testing of buried optical circuits at wafer level is key to enabling volume production and actual deployment. It is therefore desirable
10 to provide a method for in-line optical testing.

Summary of the Invention

Accordingly, in a first aspect, the present invention provides a method for in-line optical testing including providing a substrate, forming an optical device on the substrate, and forming a test circuit on the substrate, the test circuit being optically
15 coupled to the optical device. An optical test is performed on the optical device with the test circuit. The test circuit is then removed.

Other aspects and advantages of the invention will become apparent from the following detailed description, taken in conjunction with the accompanying drawings, illustrating by way of example the principles of the invention.

20 Brief Description of the Drawings

Embodiments of the invention will now be described, by way of example only, with reference to the accompanying drawings, in which:

FIGS. 1A through 1C are schematic cross-sectional views illustrating a method for in-line optical testing in accordance with an embodiment of the present
25 invention;

FIG. 2 is a schematic top plan view of an optical device and a test circuit of FIG. 1B;

FIGS. 3A through 3C are schematic cross-sectional views illustrating a method for in-line optical testing in accordance with another embodiment of the present invention;

FIG. 4 is a schematic top plan view of an optical device and a test circuit of FIG. 3A;

FIG. 5 is a schematic top plan view of an optical device and a test circuit in accordance with another embodiment of the present invention;

FIGS. 6A and 6B are schematic cross-sectional views illustrating a method for in-line optical testing in accordance with yet another embodiment of the present invention; and

FIGS. 7 and 8 are schematic cross-sectional views of an optical device and a test circuit in accordance with alternative embodiments of the present invention.

Detailed Description of Exemplary Embodiments

The detailed description set forth below in connection with the appended drawings is intended as a description of presently preferred embodiments of the invention, and is not intended to represent the only forms in which the present invention may be practiced. It is to be understood that the same or equivalent functions may be accomplished by different embodiments that are intended to be encompassed within the scope of the invention.

A method for in-line optical testing will now be described below with reference to FIGS. 1A through 1C.

Referring now to FIG. 1A, a substrate 10 is provided as shown. The substrate 10 may be a commercially available silicon-on insulator (SOI) wafer. In

the embodiment shown, the substrate 10 may be formed of silicon (Si) and may be provided with a bottom oxide layer (BOX) 12 and a crystal-silicon (crystal-Si) device layer 14.

Referring now to FIG. 1B, an optical device or device under test (DUT) 16 is
5 formed on the substrate 10 and this is followed, in the present embodiment, by deposition of a cladding layer 18. A test circuit 20 is formed on the substrate 10, the test circuit 20 being optically coupled to the optical device 16.

In the present embodiment, the optical device or DUT 16 is formed in the crystal-Si device layer 14 shown in FIG. 1A.

10 The cladding layer 18 may be formed of silicon dioxide (SiO_2).

In the embodiment shown, the test circuit 20 is at least partially formed on a waveguide layer 22. The waveguide layer 22 may be formed of silicon (Si) and/or silicon nitride (Si_3N_4). In the present embodiment, the test circuit 20 is fabricated on a different waveguide layer above a waveguide layer of the DUT 16. In one or more
15 alternative embodiments, the test circuit 20 may be fabricated on a different waveguide layer below a waveguide layer of the DUT 16 or on the same waveguide layer as the DUT 16.

Referring now to FIG. 2, a schematic top plan view of the optical device 16 and the test circuit 20 of FIG. 1B is shown. In the embodiment shown, the test
20 circuit 20 includes an inter-layer optical coupler 24 optically coupled to the optical device 16, a grating coupler 26 and a bus waveguide 28 coupling the inter-layer optical coupler 24 to the grating coupler 26. In the present embodiment, the inter-layer optical coupler 24, the connecting bus waveguide 28 and the grating coupler 26 are provided as a pair. In the embodiment shown, the grating coupler 26 is
25 configured to couple light in and out of the optical device 16 for wafer level testing and is provided on the waveguide layer 22 shown in FIG. 1B. In this manner, optical access to the DUT 16 is achieved with a dedicated test circuit.

The test circuit 20 may be formed via one or more of film deposition, photolithography patterning and etching.

Referring again to FIG. 1B, an optical test is performed on the optical device 18 with the test circuit 22. More particularly, light entering from a first grating coupler 26a is coupled into the DUT 16 through the inter-layer optical coupler 24 and then proceeds to leave through a reverse path from a second grating coupler 26b.

Referring now to FIG. 1C, the test circuit 22 is removed after in-line optical testing. This may be by performing an etching process to remove the test circuit 20 shown in FIG. 1B. In the present embodiment, a blanket etching process may be performed. More particularly, the test circuit 22 may be removed by blanket etching of the waveguide layer 22 shown in FIG. 1B. Advantageously, by removing the grating coupler 26 that is connected to the DUT 16, optical input/output (I/O) options of the optical device 16 are opened up, allowing optical access to individual components of the optical device 16.

Although not shown in the present embodiment, additional device layers may be built thereon after removal of the test circuit 22.

In the manner described above, reconfigurable in-line testing with a test circuit formed on a different waveguide layer than the DUT 16 is thus achieved.

Another method for in-line optical testing will now be described below with reference to FIGS. 3A through 3C.

Referring now to FIG. 3A, a substrate 50 is provided as shown. In the embodiment shown, the substrate 50 is provided with a bottom oxide layer (BOX) 52 and a crystal-silicon (crystal-Si) device layer 54. An optical device or device under test (DUT) 56 and a test circuit 58 are formed on the substrate 50, the test circuit 58 being optically coupled to the optical device 56.

In the embodiment shown, the test circuit 58 is formed on the same waveguide or optical layer 54 as the DUT 56 in a designated area of the substrate 50. In the present embodiment, the optical device 56 and the test circuit 58 may be simultaneously formed. Advantageously, this minimises or reduces the need for
5 extra processing steps. The DUT 56 and the test circuit 58 may be simultaneously formed in and/or on the crystal-Si device layer 54 of the substrate 50 by a two-step silicon (Si) etch process.

Different test circuits may be employed depending on the design of the optical device or DUT 56. The different test circuits may employ, for example, an
10 edge coupler, such as a nano-taper coupler or a suspended coupler, or a directional coupler (DC), depending on the design of the DUT 56.

Referring now to FIG. 4, a schematic top plan view of the optical device 56 and the test circuit 58 of FIG. 3A is shown. In the embodiment shown, the test circuit 58 includes an edge coupler 60 optically coupled to the optical device 56, a
15 grating coupler 62 and a bus waveguide 64 coupling the edge coupler 60 to the grating coupler 62. In the present embodiment, the edge coupler 60 is a nano-taper coupler and the nano-taper coupler 60, the connecting bus waveguide 64 and the grating coupler 62 are provided as a pair. In the embodiment shown, the grating coupler 62 is configured to couple light in and out of the optical device 56 for wafer
20 level testing and is provided on the waveguide layer 54 shown in FIG. 3A. In this manner, optical access to the DUT 56 is achieved with a dedicated test circuit.

Referring again to FIG. 3A, an optical test is performed on the optical device 56 with the test circuit 58. During the optical test, light is coupled into the optical device or DUT 56 through the nano-taper coupler 60.

25 Referring now to FIG. 3B, the test circuit 58 is removed after in-line optical testing is completed. This may be by performing an etching process to remove the test circuit 58 shown in FIG. 3A. In the present embodiment, a selective etching

process may be performed. More particularly, a selective silicon (Si) etch step may be performed to remove the test circuit 58.

Referring now to FIG. 3C, a cladding layer 66 may then be deposited over the optical device 56. The cladding layer 66 may be formed of silicon dioxide (SiO₂).

5 Although not shown in the present embodiment, additional device layers may be built thereon after deposition of the cladding layer 66.

In the manner described above, reconfigurable in-line testing with a test circuit formed on the same optical layer as the DUT 56 is thus achieved.

Referring now to FIG. 5, a schematic top plan view of an optical device or
10 DUT 100 and a test circuit 102 in accordance with another embodiment of the present invention is shown. In the embodiment shown, the test circuit 102 includes a directional coupler 104 optically coupled to the optical device 100, a grating coupler 106 and a bus waveguide 108 coupling the directional coupler 104 to the grating coupler 106. In the present embodiment, the directional coupler 104, the
15 connecting bus waveguide 108 and the grating coupler 106 are provided as a pair. During optical testing, light is coupled into the optical device or DUT 100 through the directional coupler 104. The test circuit 102 of the present embodiment may be employed when the optical device or DUT 100 is an isolated device or is provided with grating coupler input/output (I/O).

20 Yet another method for in-line optical testing will now be described below with reference to FIGS. 6A and 6B.

Referring now to FIG. 6A, a substrate 150 is provided and an optical device or device under test (DUT) 152 and a test circuit 154 are formed on the substrate 150, the test circuit 154 being optically coupled to the optical device 152. In the
25 embodiment shown, the substrate 150 is provided with a bottom oxide layer (BOX) 156.

The test circuit 154 in the present embodiment is designed to be reconfigurable by a subsequent fabrication process step. In the present embodiment, the test circuit 154 includes a directional coupler with a different coupling coefficient under different clad conditions that is optically coupled to the optical device. Such a coupler may have a maximum optical coupling coefficient to the DUT in air cladding for in-line testing. The directional coupler may be connected to a grating coupler via a bus waveguide and may be an asymmetrical direction coupler. The asymmetrical direction coupler may have a different width to the DUT as shown in FIG. 6A, a different height to the DUT as shown in FIG. 7 or both as shown in FIG. 8.

Referring now to FIG. 6B, the test circuit 154 is removed by reconfiguring the test circuit 154. In the present embodiment, a cladding layer 158 is deposited over the test circuit 154 to reconfigure the test circuit 154 as after cladding deposition, the coupling coefficient of the directional coupler drops to a minimum, disabling optical access to the DUT 152. Removal of the test circuit 154 is thus achieved by configuring the test circuit 154 to cut off optical access to the optical device 152 after performing in-line optical testing.

In the manner described above, reconfigurable in-line testing with a reconfigurable test circuit 154 is thus achieved.

As is evident from the foregoing discussion, the present invention provides a method for reconfigurable in-line optical testing of photonic integrated circuits and devices on a semiconductor wafer, after which the in-line optical testing circuits may be removed or reconfigured. Advantageously, in-line optical testing of photonic integrated circuits and devices on a semiconductor wafer provides for economics of scale in volume scale-ups. Further advantageously, this also allows optical devices to be tested as soon as possible after formation during the fabrication process and this facilitates early failure detection for repair or scratch.

While preferred embodiments of the invention have been illustrated and described, it will be clear that the invention is not limited to the described embodiments only. Numerous modifications, changes, variations, substitutions and equivalents will be apparent to those skilled in the art without departing from the
5 scope of the invention as described in the claims.

Further, unless the context clearly requires otherwise, throughout the description and the claims, the words "comprise", "comprising" and the like are to be construed in an inclusive as opposed to an exclusive or exhaustive sense; that is to say, in the sense of "including, but not limited to".

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CLAIMS

1. A method for in-line optical testing, comprising:
providing a substrate;
5 forming an optical device on the substrate;
forming a test circuit on the substrate, wherein the test circuit is optically coupled to the optical device;
performing an optical test on the optical device with the test circuit; and
removing the test circuit.
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2. The method of claim 1, wherein the step of removing the test circuit comprises performing an etching process to remove the test circuit.
3. The method of claim 2, wherein the etching process is one of a selective
15 etching process and a blanket etching process.
4. The method of claim 1, wherein the step of removing the test circuit comprises reconfiguring the test circuit.
- 20 5. The method of claim 4, wherein the step of reconfiguring the test circuit comprises depositing a cladding layer over the test circuit to reconfigure the test circuit.
6. The method of claim 1, wherein the optical device and the test circuit are
25 simultaneously formed.
7. The method of claim 1, wherein the test circuit comprises a coupler that is optically coupled to the optical device, wherein the coupler is one of an inter-layer optical coupler, an edge coupler and a directional coupler.

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8. The method of claim 7, wherein the edge coupler comprises one of a nano-taper coupler and a suspended coupler.
9. The method of claim 7, wherein the directional coupler comprises an asymmetrical direction coupler.
10. The method of claim 9, wherein the asymmetrical directional coupler has at least one of a different height and a different width than the optical device.
- 10 11. The method of claim 7, wherein the test circuit further comprises:
 - a grating coupler; and
 - a bus waveguide coupling the coupler to the grating coupler.