

ABSTRACT

**BIDIRECTIONAL BUFFER WITH
LATCH AND PARITY CAPABILITY**

A circuit for buffering and parity checking digital data communicated between first and second data buses includes a plurality of bidirectional bit buffer circuits. Each of the bidirectional bit buffer circuits includes : a first data path comprising a data receiver, latch, and driver connected in series between the first and second data buses, respectively; a second data patch comprising a data receiver, latch and driver connected in series between the second and first data buses, respectively; control mechanism for controlling the drivers to selectively place the output of the drivers in an active driving or high impedance state; and control mechanisms for controlling the data latches to selectively latch or pass through data. A parity generating circuit is connected at the output of the latch in the first data path of each of the bidirectional bit buffer circuits for generating a parity bit responsive to the data at the output of these latches. A transparent and driver circuit with phase splitter are provided for increasing the speed of the circuit without substantially increasing the power requirements.

Fig. : 2

This Sheet Has Been Replaced

