Abstract

A CMOS GATE ARCHITECTURE FOR INTEGRATION OF SALICIDE PROCESS IN SUB 0.1μM DEVICES

A method to form a "mushroom shaped" gate structure 18 22 44A 70 that increases the top gate silicide contact area and improves the salicide process, especially $TiSi_2$ salicide. The novel upper gate extensions 44A increase the top gate surface area so that the silicide gate contacts 70 will have a low resistivity. The invention includes forming a gate stack 18 22 26 comprised of a gate oxide layer 18, a center gate portion 22 and a hard mask 26. Next, we form a first insulating layer 40 over the gate stack 22 26 18. The hard mask 26 and a first thickness of the first insulating layer 40 are removed to expose sidewalls of the center gate portion 22. A second conductive layer 44 is formed over the first insulating layer 46 and the center gate portion 22. The second conductive layer 44 is etched to form critical rounded upper gate extensions 44A on the sidewalls of the center gate portion 22. Lower rectangular sidewall spacers 52 are formed on the sidewalls of the center gate portion 22. Source/drain regions 54 are formed. A salicide process forms silicide source/drain contacts 64 and forms extra large silicided gate contacts 70 to reduce parasitic resistance.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)