

1/8

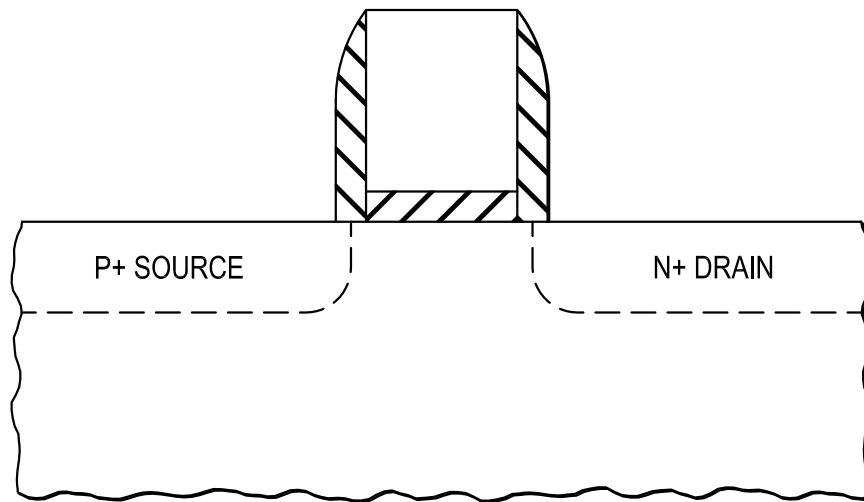


FIG. 1A
(PRIOR ART)

FIG. 1B
OFF STATE
TUNNELING IS
NOT ALLOWED

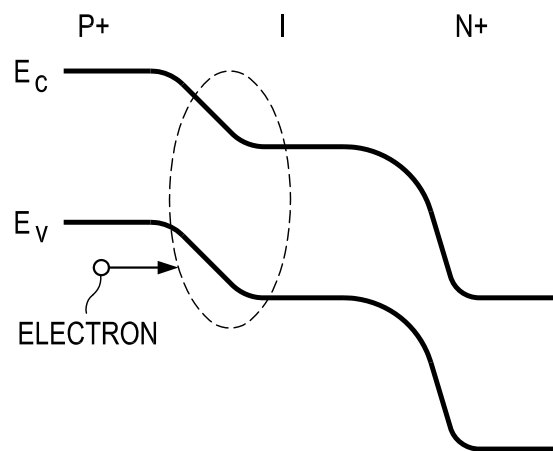
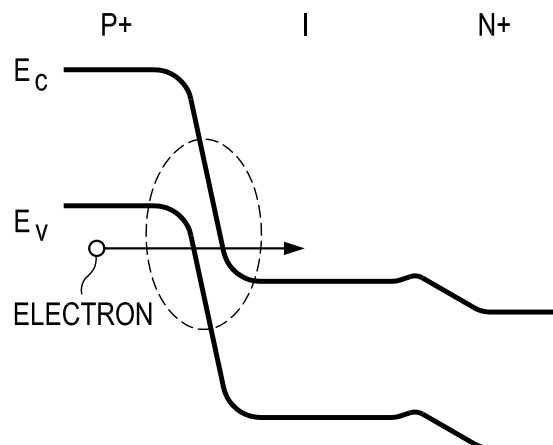


FIG. 1C
ON STATE
TUNNELING IS
ALLOWED



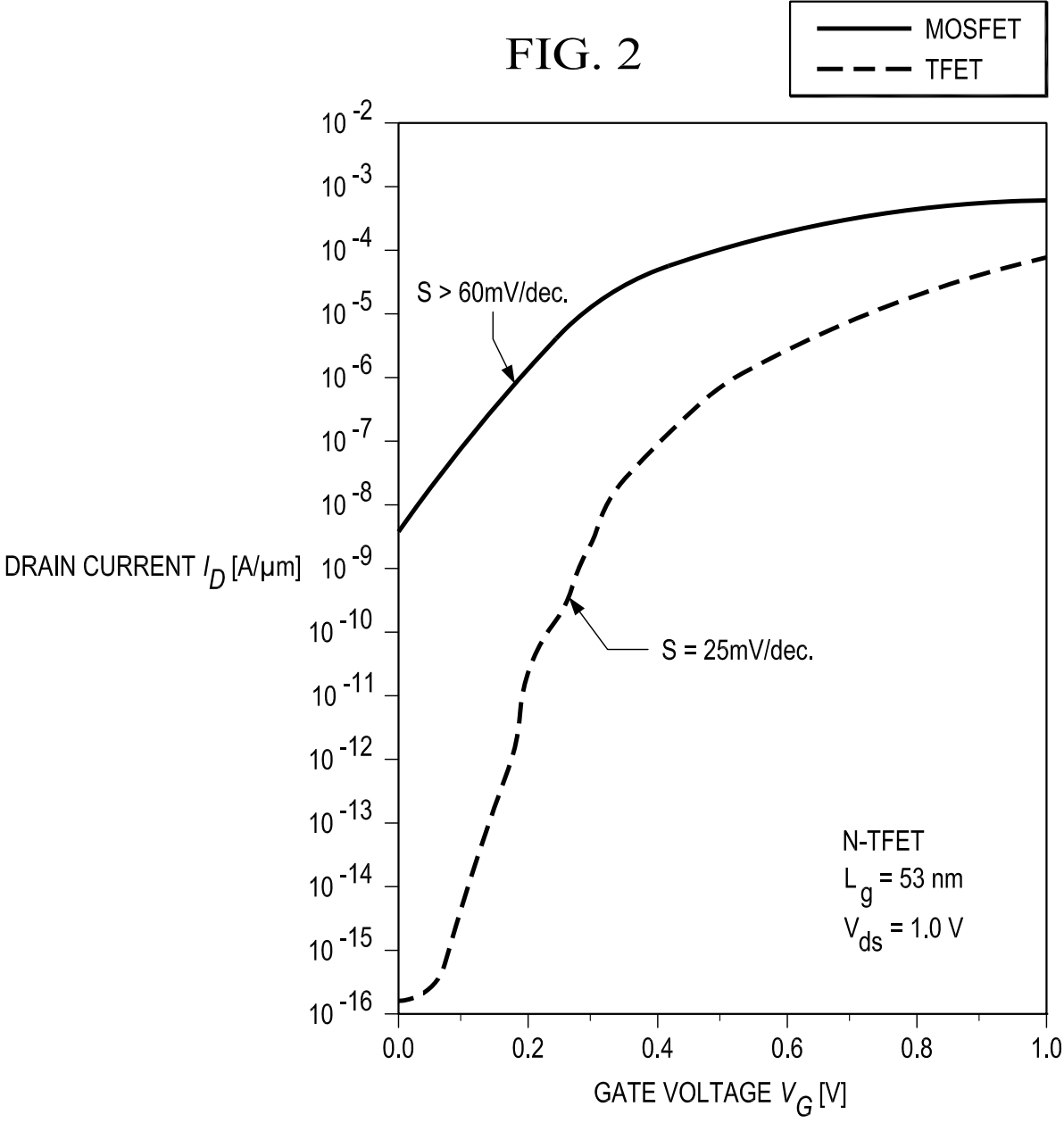


FIG. 3A
ON-STATE OF A
N-CHANNEL TFET

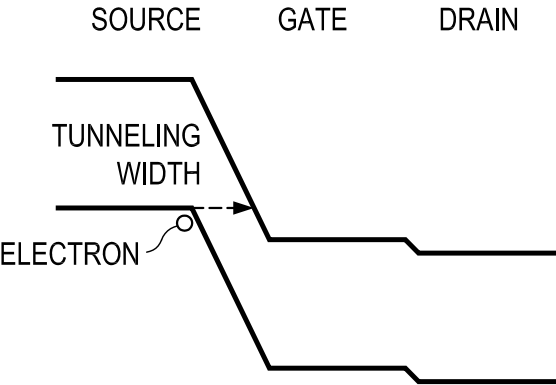


FIG. 3B

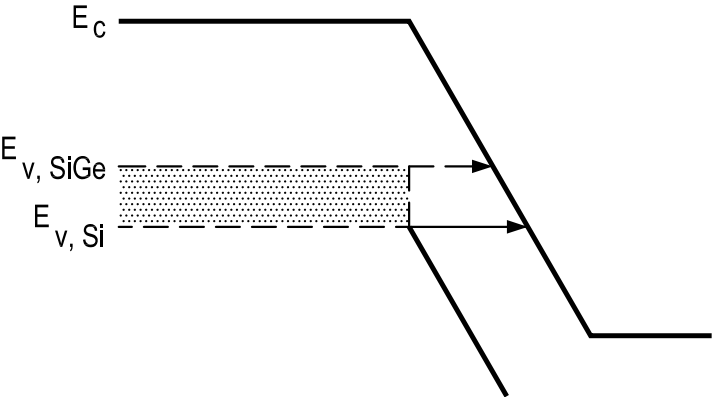
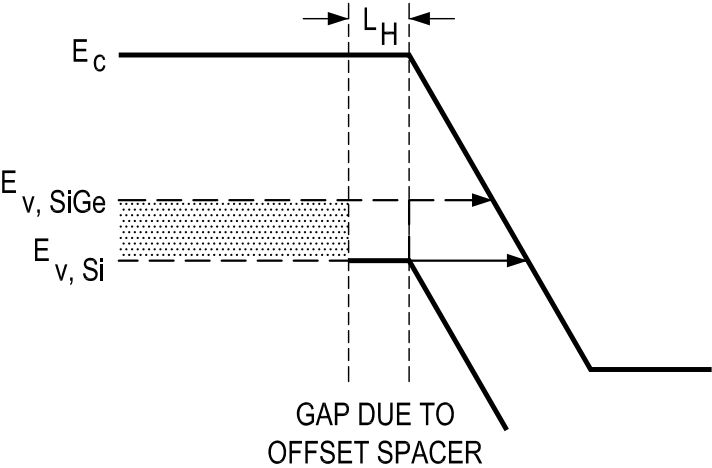


FIG. 3C



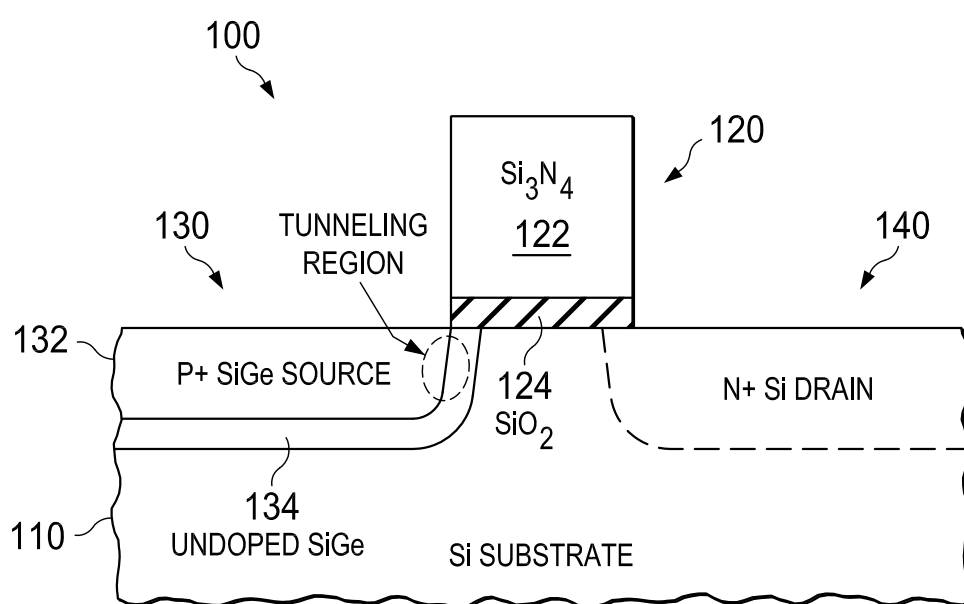


FIG. 4

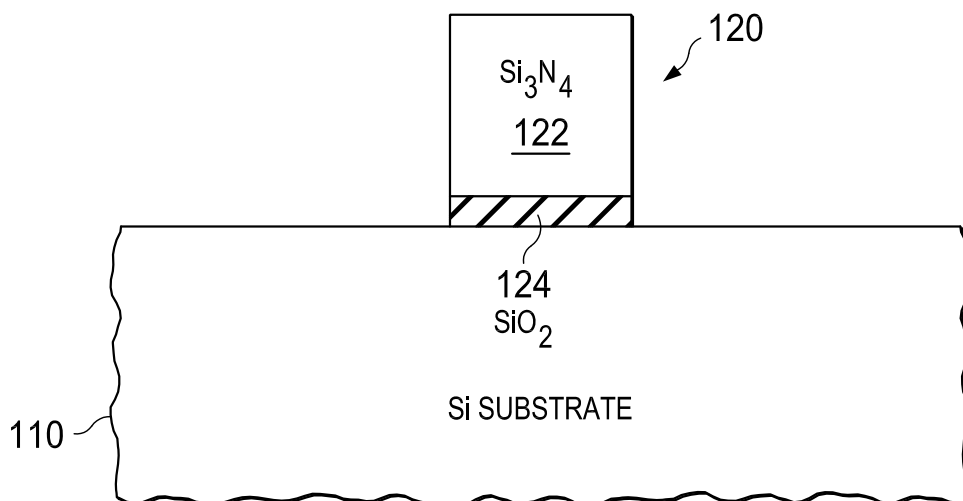


FIG. 5A

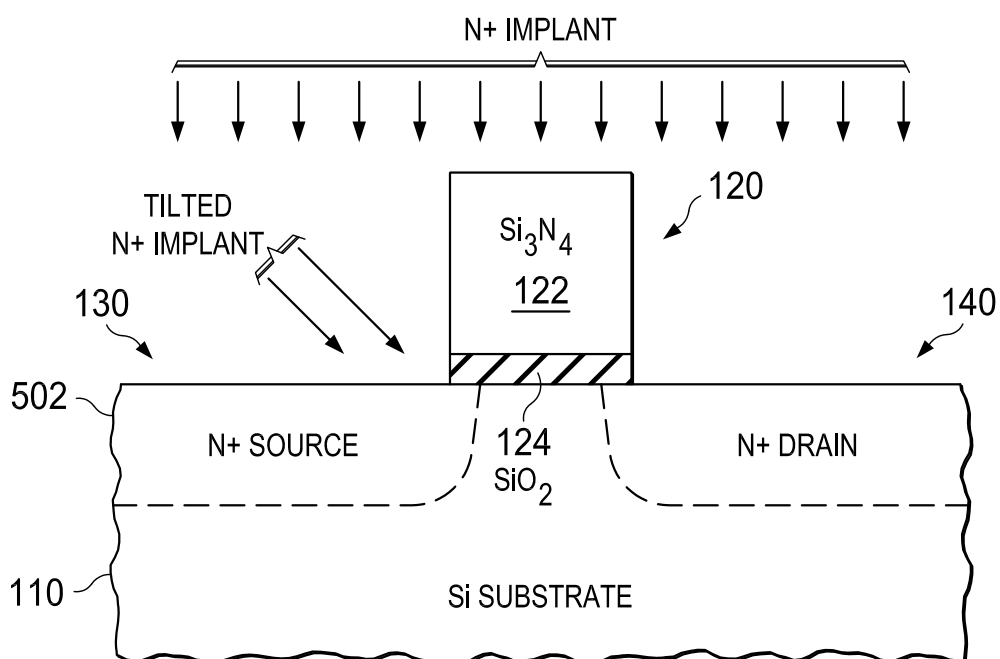


FIG. 5B

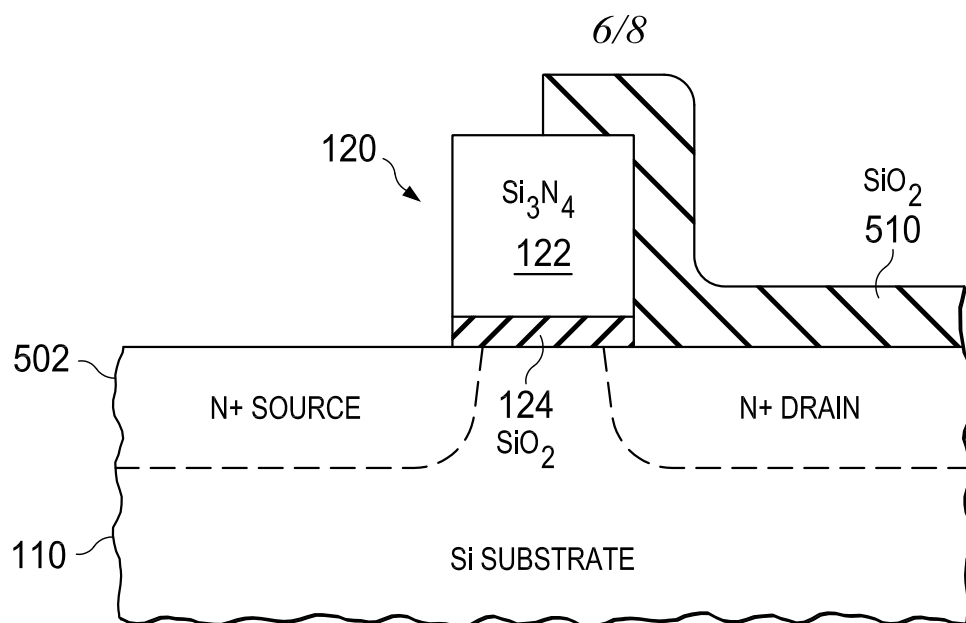


FIG. 5C

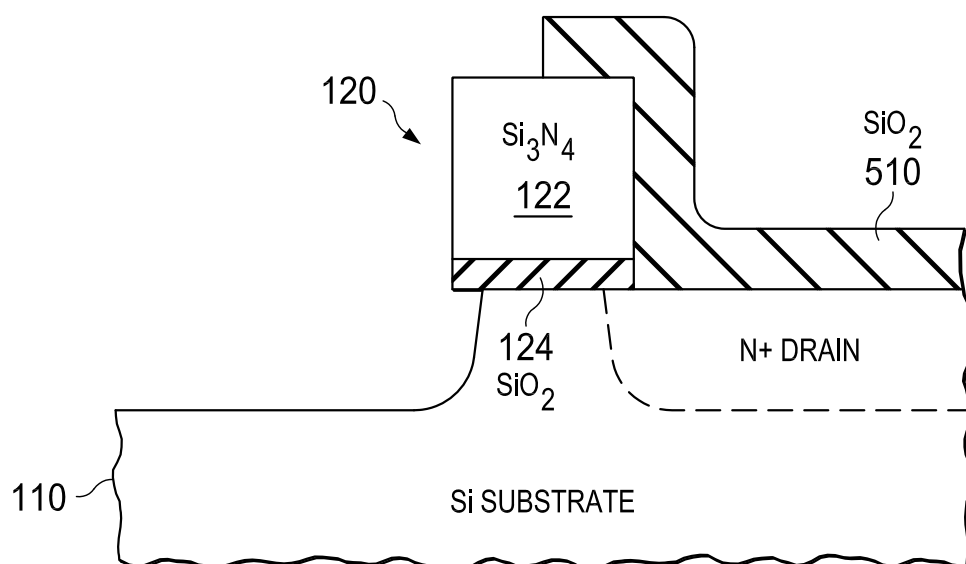


FIG. 5D

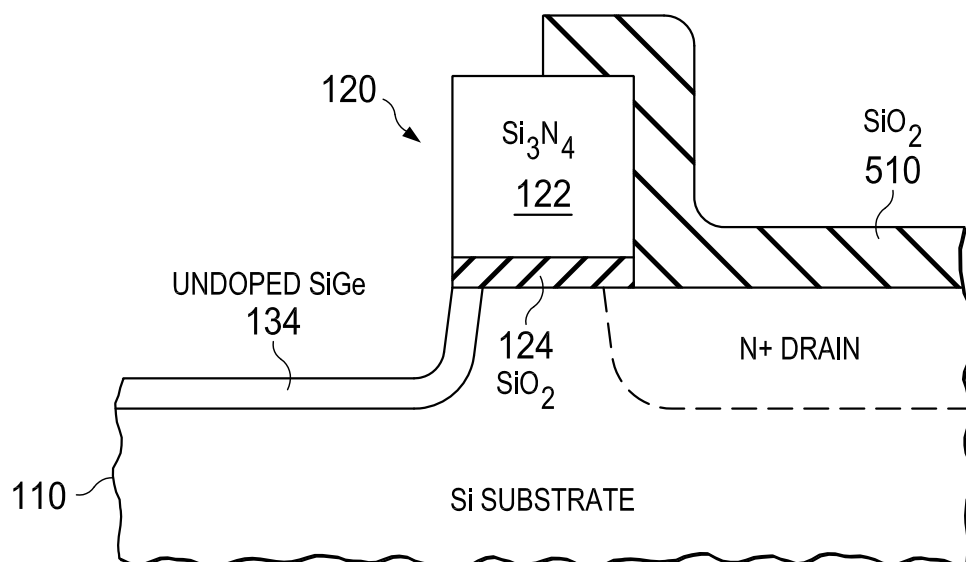


FIG. 5E

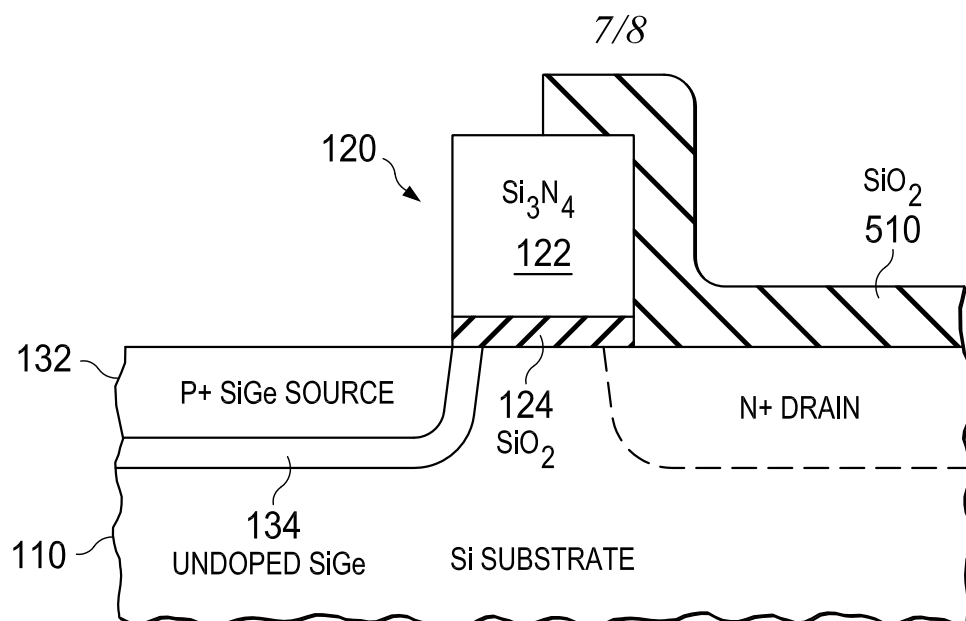


FIG. 5F

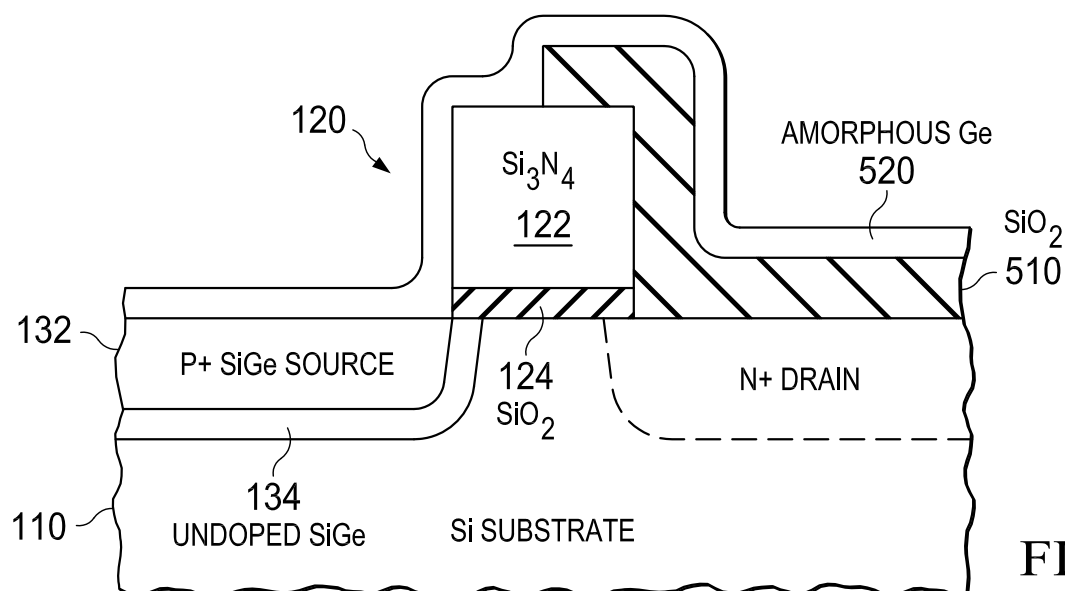


FIG. 5G

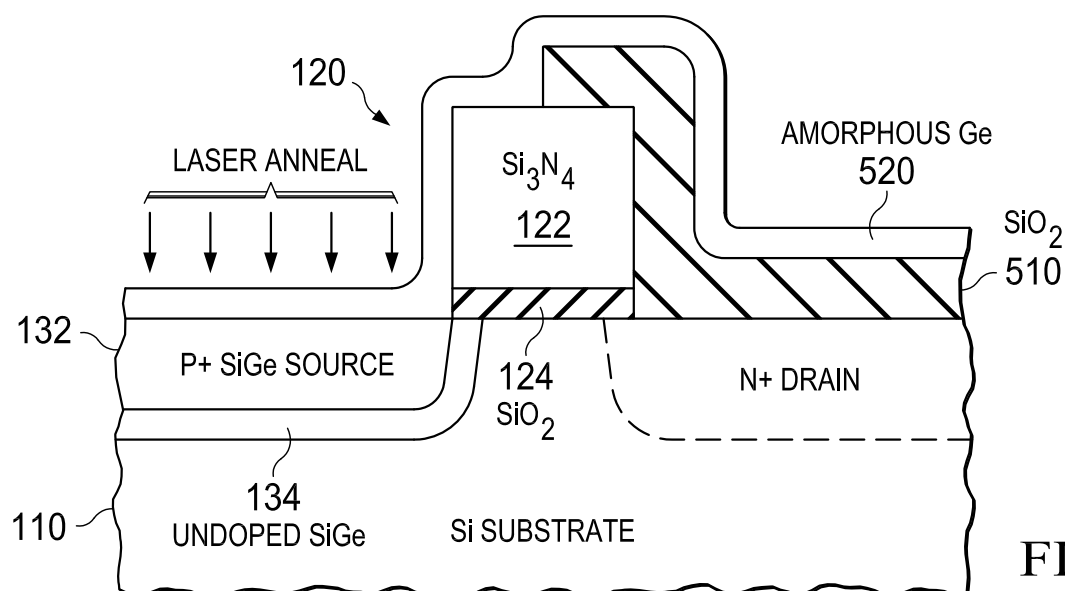


FIG. 5H

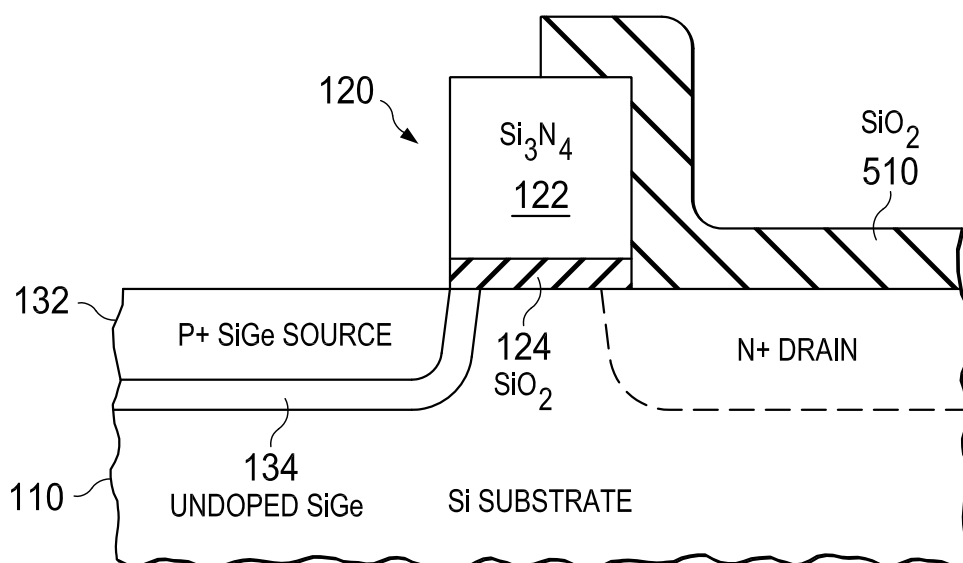


FIG. 5I

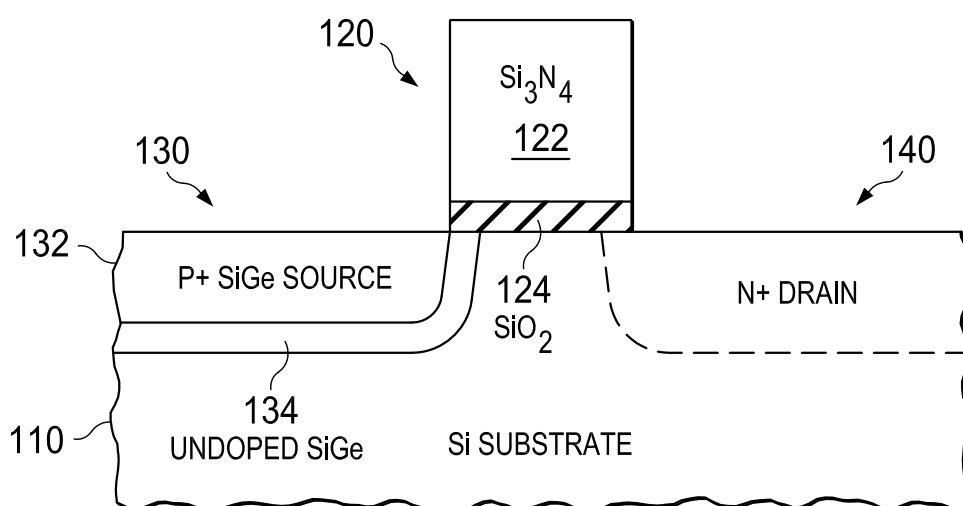


FIG. 5J