

Method of Manufacturing Silicon Single Crystal, Silicon Single Crystal, and Wafer

Technical Field

The present invention relates to a method of manufacturing silicon single crystal, a silicon single crystal, and a wafer, and particularly to a method of manufacturing silicon single crystal with a Czochralski method, a silicon single crystal, and a wafer.

Background Art

A power device mounted on cars, home appliances or the like should have a high withstand voltage, and resistance of a substrate affects characteristics thereof. Therefore, a silicon wafer used as the substrate is required to be high in resistivity and less in variation thereof.

When a p-type silicon single crystal is grown with a Czochralski method with boron being added as an impurity, boron is condensed in a silicon melt during growth of single crystal, because a segregation coefficient of boron with respect to silicon single crystal is less than 1. Then, boron concentration in silicon single crystal increases with growth of single crystal. Consequently, resistivity of silicon single crystal is varied at tip and rear ends of a central axis during crystal growing (hereinafter referred to as a "central axis during crystal growing") of obtained silicon single crystal (ingot).

As a conventional technique for suppressing such variation in resistivity due to segregation, a technique

for suppressing variation in resistivity in a direction of crystal growth by adding phosphorus corresponding to 25 to 30 % of boron concentration to the initial silicon melt and growing crystal with the Czochralski method is available. Japanese Patent No. 3931956 refers to this conventional technique.

Problems to Be Solved by the Invention

The conventional technique above, however, cannot realize stricter radial uniformity of resistivity and variation in resistivity among wafers, that are required in a silicon single crystal wafer for power device applications.

The present invention was made to solve such a problem.

Means for Solving the Problems

The problem above of the present invention is solved by the following method.

A method of manufacturing silicon single crystal, characterized in that p-type silicon single crystal is grown with a Czochralski method from an initial silicon melt in which a boron concentration is not higher than 4×10^{14} atoms/cm³ and a ratio of phosphorus concentration to boron concentration is not lower than 0.42 and not higher than 0.50.

Effects of the Invention

A p-type silicon single crystal, from which a wafer having high resistivity, good radial uniformity of

resistivity and less variation in resistivity can be obtained, can be manufactured with a Czochralski method.

Brief Description of the Drawings

Fig. 1 is a schematic diagram of a silicon single crystal manufacturing apparatus for performing a method of manufacturing silicon single crystal according to an embodiment of the present invention.

Fig. 2 is a flowchart for performing the method of manufacturing silicon single crystal according to the embodiment of the present invention.

Fig. 3 is a diagram showing a result of simulation of relation between a solidified fraction of silicon single crystal and an impurity concentration in silicon single crystal as well as a result of measurement and a result of simulation of relation between a solidified fraction and resistivity of silicon single crystal.

Fig. 4 is a diagram showing a result of simulation of dependency on an initial silicon melt P/B ratio of relation between a solidified fraction and resistivity of silicon single crystal.

Fig. 5 is an illustrative view showing a silicon solid-liquid interface at the time of growing silicon single crystal with a Czochralski method and the relation between a position on a central axis during crystal growing and resistivity.

Modes for Carrying Out the Invention

A method of manufacturing silicon single crystal, a silicon single crystal, and a wafer according to an embodiment of the present invention will be described

hereinafter in detail with reference to the drawings.

A method of manufacturing silicon single crystal according to the present embodiment relates to manufacturing of a wafer for a power device.

A wafer employed for forming a power device should satisfy such specifications as resistivity not lower than 50 $\Omega\cdot\text{cm}$, variation in resistivity among wafers not higher than 10 %, and radial variation in resistivity in wafer not higher than 3 %, mainly for the following reasons.

First, since a high voltage is applied to a power device, the power device should have a high withstand voltage. In addition, a withstand voltage of a power device correlates with a value of resistivity of a wafer with which the power device is formed. Therefore, a wafer employed for a power device should have high resistivity. Currently prevailing power devices have a withstand voltage not lower than 250 V, and a wafer is required to have resistivity not lower than 50 Ωcm . On the other hand, as resistivity of a wafer becomes higher, a width of a depletion layer becomes greater. A width of a depletion layer excessively larger than a device structure will lead to contact of the depletion layer with a portion other than pn junction and resulting lowering in withstand voltage characteristics. From the foregoing, in order to increase a withstand voltage of a power device, resistivity of a wafer should be higher and at the same time, variation thereof should be less.

Secondly, in a power device, a transistor in which a collector current is extracted from a back surface of a silicon substrate (for example, an IGBT (Insulated Gate

Bipolar Transistor)) is provided, and influence by variation in resistivity in wafer on characteristics of a transistor is relatively large. Therefore, a wafer for forming such a transistor should be a wafer having high resistivity and less variation such that characteristics of the transistor are within the specifications.

Thirdly, radial variation in resistivity in wafer leads to low yield in screening after formation of a device, because a device manufacturer cannot screen wafers at the time of accepting the same. Therefore, in order to suppress increase in cost due to lower yield of devices, a wafer to be used for a device should have less variation in resistivity.

Fig. 1 is a schematic diagram of a silicon single crystal manufacturing apparatus for performing a method of manufacturing silicon single crystal according to the present embodiment.

As shown in Fig. 1, a silicon single crystal manufacturing apparatus 100 is an apparatus for manufacturing silicon single crystal with a Czochralski method (hereinafter referred to as a "CZ method"). Silicon single crystal manufacturing apparatus 100 has a crucible 30 accommodating a silicon melt and a drive device 10 moving up and down silicon single crystal 2, rotating silicon single crystal 2 and rotating crucible 30. Silicon single crystal manufacturing apparatus 100 has a control device 1 for controlling moving up and down of silicon single crystal 2, rotation of silicon single crystal 2, and rotation of crucible 30 by drive device 10.

Silicon single crystal manufacturing apparatus 100

has a chamber 20 accommodating crucible 30 and silicon single crystal 2, a heater 42 arranged along a sidewall of crucible 30, a heater 44 arranged under crucible 30, and a heat insulator 26 arranged along a sidewall and a bottom of chamber 20.

Silicon single crystal manufacturing apparatus 100 has a wire 3 suspended from an upper portion of chamber 20 and a chuck 6 provided at a tip end of wire 3, for holding seed crystal 8.

Silicon single crystal manufacturing apparatus 100 has a gas introduction port 22 for introducing an inert gas into chamber 20, a gas exhaust port 24 for exhausting the introduced inert gas out of chamber 20, and a flow regulation tube 60 for regulating flow of the inert gas. An Ar gas is exemplified as an inert gas.

A silicon melt 32 is provided from polycrystalline silicon as a source material.

In the present embodiment, in order to manufacture p-type silicon single crystal 2, boron (B) is added as a p-type impurity (acceptor) to silicon melt 32 from which the single crystal initially grows (hereinafter referred to as an "initial silicon melt"). In addition, phosphorus (P), which is an n-type impurity (donor) and lower than boron in segregation coefficient with respect to silicon single crystal 2, is further added. Thus, the reason why phosphorus which is an impurity opposite to boron in conductivity type and lower than boron in segregation coefficient with respect to silicon single crystal 2 is added to the initial silicon melt is to increase resistivity of silicon single crystal 2 and to prevent variation in resistivity in a direction of the central

axis during crystal growing (increase in a rate of change in resistivity).

In addition, in the present embodiment, variation in resistivity in the direction of the central axis during crystal growing is further suppressed in order to further suppress radial variation in resistivity (increase in a rate of change in resistivity) in a plane perpendicular to the central axis during crystal growing of silicon single crystal 2. To that end, the initial silicon melt is made to satisfy that the boron concentration is not higher than 4×10^{14} atoms/cm³ and a ratio of phosphorus concentration to the boron concentration is not lower than 0.42 and not higher than 0.50, details of which will be described later.

Crucible 30 is formed, for example, of synthetic quartz glass. Crucible 30 is connected at its bottom to a shaft 34 supporting the crucible. Flow regulation tube 60 is provided above crucible 30 and it is substantially in a shape of a frustum.

Drive device 10 comprises a winding machine 12 for pulling out and winding up wire 3 and a crucible driver 14 for rotating crucible 30. Winding machine 12 can wind up wire 3 as it turns. Shaft 34 is connected to crucible driver 14 and crucible 30 is rotated by crucible driver 14 with shaft 34 being interposed.

Control device 1 is electrically connected to winding machine 12, heaters 42 and 44, and crucible driver 14. Control device 1 can control a speed of wind-up of wire 3 by winding machine 12, a direction of rotation of wire 3, a speed of rotation of wire 3, that is, a speed of crystal growing of silicon single crystal 2, a direction of rotation of silicon single crystal 2, and a speed of

rotation of silicon single crystal 2. Control device 1 can control a direction and a speed of rotation of crucible 30 by crucible driver 14. Control device 1 can control output of heaters 42 and 44 and can control a temperature of silicon melt 32 by fixing the output of heater 44 and varying the output of heater 42.

Control device 1 is mainly configured with a CPU (Central Processing Unit) and a storage device, and it causes the storage device to store an operation of entire silicon single crystal manufacturing apparatus 100. Control device 1 can be configured, for example, with a PC (Personal Computer) or an EWS (Engineering Work-Station). The method of manufacturing silicon single crystal according to the present embodiment can be performed as control device 1 controls an operation of each component.

Fig. 2 is a flowchart for performing the method of manufacturing silicon single crystal according to the present embodiment.

The method of manufacturing silicon single crystal according to the present embodiment is a method for manufacturing silicon single crystal 2 with the CZ method, and it comprises an inert gas filling step S1 of setting an inert gas atmosphere in chamber 20, a melt generation step S2 of generating silicon melt 32, a silicon single crystal growth step S3 of growing silicon single crystal 2, and a separation step S4 of separating silicon single crystal 2 from silicon melt 32.

In inert gas filling step S1, chamber 20 is sealed and chamber 20 is set to the inert gas atmosphere by introducing an inert gas through gas introduction port 22 while a gas is evacuated from the chamber through gas

exhaust port 24 by means of a vacuum pump (not shown). It is noted that chamber 20 is maintained in the inert gas atmosphere by feeding the inert gas into chamber 20 also in each step which will be described below.

In melt generation step S2 after inert gas filling step S1, the source material supplied into crucible 30 is molten by heaters 42 and 44, to thereby generate initial silicon melt 32.

In the present embodiment, boron and phosphorus are added to silicon melt 32, so that initial silicon melt 32 satisfies that the boron concentration is not higher than 4×10^{14} atoms/cm³ and a ratio of phosphorus concentration to the boron concentration is not lower than 0.42 and not higher than 0.50.

As initial silicon melt 32 has such composition, resistivity of silicon single crystal 2 can be increased, a rate of change in resistivity along a central axis during crystal growing L1 can further be lowered, and a rate of change in resistivity in a cross-section perpendicular to central axis during crystal growing L1 can be lowered. Namely, p-type silicon single crystal 2, in which resistivity along central axis during crystal growing L1 is not lower than $50 \Omega \cdot \text{cm}$, a rate of change in resistivity along central axis during crystal growing L1 is not higher than 10 %, and a rate of change in resistivity in the cross-section perpendicular to central axis during crystal growing L1 is not higher than 3 %, can be grown.

Here, a rate of change in resistivity is defined by Equation (1) below.

Rate of Change in Resistivity = (Maximum Value of

Resistivity - Minimum Value of Resistivity) / Maximum
Value of Resistivity Equation (1)

In silicon single crystal growth step S3 after melt generation step S2, seed crystal 8 is moved down to a surface of silicon melt 32 by means of winding machine 12 and it is immersed therein. Then, silicon single crystal 2 is grown from silicon melt 32 by means of winding machine 12, to thereby grow a straight part of ingot 4 of silicon single crystal 2. Silicon single crystal 2 and crucible 30 rotate in a direction opposite to each other.

In the present embodiment, a speed of growing silicon single crystal 2 in silicon single crystal growth step S3 is not lower than 0.9 mm/min and a rate of cooling of a crystal edge portion can be at least 1.4 times as high as a rate of cooling of a crystal central portion. Here, the rate of cooling refers to a value calculated by multiplying an average temperature gradient (°C/mm) in a direction of an axis of crystal growth from the melting point to 1350°C, which is an average in a range from the melting point to 1350°C during crystal growth, by a rate of crystal growing (mm/min). A rate of crystal growing lower than 0.9 mm/min is not preferred because of poor productivity. A rate of cooling of a crystal edge portion less than 1.4 times as high as the rate of cooling of a crystal central portion leads to poor efficiency in cooling silicon single crystal, and thus a rate of crystal growing becomes lower than 0.9 mm/min and productivity becomes poor. The upper limit of a rate of crystal growing is 1.9 mm/min in consideration of the capability of a silicon single crystal growing apparatus that can be realized, and the upper limit of a rate of cooling of the

crystal edge portion is twice as high as the rate of cooling of the crystal central portion.

Straight part of ingot 4 is a cylindrical portion of silicon single crystal 2, of which diameter is substantially constant in a direction of central axis during crystal growing L1 of silicon single crystal 2. Once silicon single crystal 2 reaches a diameter set in advance after a conical portion is formed, straight part of ingot 4 is grown.

In separation step S4 after straight part of ingot 4 is grown, wind-up of wire 3 is stopped and silicon single crystal 2 is separated from silicon melt 32 by moving down crucible 30.

According to the present embodiment, p-type silicon single crystal 2, in which resistivity along central axis during crystal growing L1 is not lower than $50\ \Omega\cdot\text{cm}$, a rate of change in resistivity along central axis during crystal growing L1 is not higher than 10 %, and a rate of change in resistivity in the cross-section perpendicular to central axis during crystal growing L1 is not higher than 3 %, can be manufactured.

The reason why the present embodiment achieves such an effect will be described below.

Fig. 3A is a diagram showing a result of simulation of relation between a solidified fraction of silicon single crystal and an impurity concentration in silicon single crystal. Fig. 3B is a diagram showing a result of measurement and a result of simulation of relation between a solidified fraction and resistivity of silicon single crystal. A dotted line in Fig. 3B shows a result of actual measurement, while a solid line shows a result of

simulation.

As shown in Fig. 3A, in a case where boron alone was added to the initial silicon melt, as silicon single crystal grows (that is, a solidified fraction becomes higher), impurity concentration in silicon single crystal exponentially increases. Consequently, as shown in Fig. 3B, as silicon single crystal grows, resistivity of silicon single crystal lowers.

This is because a segregation coefficient k of boron with respect to silicon single crystal is around 0.78, which is less than 1, and therefore, as silicon single crystal grows, condensation of boron in the silicon melt proceeds and a ratio of boron taken into silicon single crystal becomes higher.

In a case where phosphorus alone was added to the initial silicon melt as well, similarly, as silicon single crystal grows, impurity concentration in silicon single crystal exponentially increases. On the other hand, segregation coefficient k of phosphorus with respect to silicon single crystal is around 0.38, which is lower than the segregation coefficient of boron. Therefore, a rate (speed) of condensation of phosphorus in the silicon melt with growth of silicon single crystal is higher than in the case of boron. Thus, a rate of lowering in resistivity with growth of silicon single crystal is also higher than in the case where boron is added.

Since boron is a p-type impurity, addition of boron to silicon single crystal produces holes as p-type carriers in silicon single crystal. Since phosphorus is an n-type impurity, addition of phosphorus to silicon single crystal produces electrons as n-type carriers in silicon

single crystal.

In silicon single crystal to which boron and phosphorus were added, produced carriers opposite to each other in conductivity type cancel each other. Therefore, by adding phosphorus together with boron to silicon single crystal in manufacturing a p-type semiconductor, p-type carrier density in silicon single crystal can be lowered and resistivity can be increased.

In addition, a rate of increase in impurity concentration with growth of silicon single crystal is greater in the case of addition of phosphorus than in the case of addition of boron. Therefore, by canceling increase in p-type carrier density by increase in boron concentration with growth of silicon single crystal by increasing n-type carrier density by increase in phosphorus concentration, lowering in resistivity with growth of silicon single crystal can be prevented. Namely, by setting a ratio of phosphorus concentration to boron concentration in the initial silicon melt (hereinafter referred to as a "P/B ratio") to an appropriate value, lowering in resistivity with growth of silicon single crystal can be prevented. Since concentration of boron and phosphorus added to the initial silicon melt is sufficiently low, boron and phosphorus are considered to independently be segregated with respect to silicon single crystal.

Specifically, as shown in Fig. 3A, by selecting a P/B ratio of the initial silicon melt such that difference between boron concentration and phosphorus concentration in silicon single crystal in a process of growth of silicon single crystal is constant, a value of resistivity

with growth of silicon single crystal can be maintained constant as shown in Fig. 3B.

Fig. 3B shows a result of measurement and a result of simulation of resistivity in a case where an initial silicon melt satisfies boron concentration of $1.6\text{E}14$ atoms/cm³ and a P/B ratio of 0.45.

Fig. 4 is a diagram showing a result of simulation of dependency on an initial silicon melt P/B ratio of relation between a solidified fraction and resistivity of silicon single crystal. Here, a ratio of resistivity in Fig. 4 is shown in the following Equation (2).

Ratio of Resistivity = (Resistivity at Certain Solidified Fraction - Minimum Value of Resistivity of That Crystal) / Maximum Value of Resistivity of That Crystal

Equation (2)

According to the simulation result shown in Fig. 4, it can be seen that, when a solidified fraction is restricted to 0 to 0.80, a rate of change in resistivity along the central axis during crystal growing can be lowered to 10 % or less, by setting the P/B ratio of the initial silicon melt to 0.42 to 0.55. As will be described later, however, in order to lower a rate of change in resistivity in a cross-section perpendicular to the central axis during crystal growing, the P/B ratio should be set to 0.42 to 0.50. The reason why the solidified fraction is restricted to 0 to 0.80 will also be described later.

Here, when the initial silicon melt has the P/B ratio from 0.42 to 0.50, such a phenomenon that resistivity of silicon single crystal 2 starts to increase around the

solidified fraction of 0.7 as silicon single crystal 2 grows (hereinafter, a point where the resistivity starts to increase being referred to as a "flexion point"). This phenomenon indicates that p-type carriers (holes) in silicon single crystal 2 started to decrease, which is caused by the fact that a rate of increase of phosphorus in silicon single crystal 2 exceeded a rate of increase of boron.

In the present embodiment, the rate of change in resistivity along the central axis during crystal growing is lowered by going so far as to produce a flexion point. Silicon single crystal after the flexion point is produced also maintains the p conductivity type so long as phosphorus concentration in silicon single crystal does not exceed boron concentration, and no problem arises in using silicon single crystal for a wafer for a power device.

By thus further lowering the rate of change in resistivity along the central axis during crystal growing, the rate of change in resistivity in the cross-section perpendicular to the central axis during crystal growing can further be lowered. The reason therefor will be described below.

Fig. 5 is an illustrative view showing a silicon solid-liquid interface (a boundary surface between the silicon melt and the silicon single crystal) at the time of crystal growing of silicon single crystal with the CZ method.

As shown in Fig. 5, a silicon solid-liquid interface at the time of crystal growing of silicon single crystal 2 has a shape protruding in a direction of central axis

during crystal growing L1 of silicon single crystal 2. A point A indicates an intersection between current solid-liquid interface and central axis during crystal growing L1. A point B' indicates an intersection between a horizontal cross-section (cross-section perpendicular to the central axis during crystal growing) of the silicon single crystal including point A and a side surface of silicon single crystal 2. A point B indicates an intersection between past solid-liquid interface and central axis during crystal growing L1. A distance between A and B is denoted as ΔZ and difference in resistivity between A and B is denoted as ΔR .

Here, since each resistivity on solid-liquid interface is constant, resistivity is the same at point B and point B'. On the other hand, change in resistivity between point A and point B corresponds to a rate of change in resistivity along central axis during crystal growing L1, while change in resistivity between point A and point B' corresponds to a rate of change in resistivity in a cross-section A1 perpendicular to central axis during crystal growing L1. Therefore, in order to lower a rate of change in resistivity in cross-section A1 perpendicular to central axis during crystal growing L1, inclination of resistivity $\Delta R/\Delta Z$ in the direction of central axis during crystal growing L1 should be lessened. Based on the simulation in Fig. 4, in order to lessen inclination of resistivity, it is effective to set the upper limit of the solidified fraction and to set a P/B ratio within a certain range. A region where the solidified fraction exceeds 0.80 has great inclination of resistivity at any P/B ratio, and therefore a rate of

change in resistivity in a cross-section perpendicular to central axis during crystal growing L1 exceeds 3 %. When the solidified fraction is restricted to 0 to 0.80, by setting the P/B ratio in the initial silicon melt between 0.42 or higher and 0.50 or lower, a rate of change in resistivity in the cross-section perpendicular to central axis during crystal growing L1 is 3 % or lower, as demonstrated in the examples which will be described later. More preferably, by setting the P/B ratio between 0.42 or higher and 0.47 or lower in a case where the solidified fraction is restricted to 0 to 0.80, the rate of change in resistivity in the cross-section perpendicular to the central axis during crystal growing is 2 % or lower as demonstrated in the examples which will be described later. In a case where the solidified fraction is restricted to 0 to 0.80, by setting the P/B ratio between more than 0.50 and 0.55 or lower, inclination of resistivity on a crystal bottom side becomes great and hence a rate of change in resistivity in the cross-section perpendicular to central axis during crystal growing L1 exceeds 3 %. By restricting the solidified fraction to less than 0.80, a rate of change in resistivity in the cross-section perpendicular to central axis during crystal growing L1 can be not higher than 3 % even though the P/B ratio is higher than 0.50 and not higher than 0.55. Restriction of the solidified fraction to less than 0.80, however, is not preferred because of poor productivity.

In order to lower a rate of change in resistivity in a cross-section perpendicular to the central axis during crystal growing, it is also effective to control

conditions for cooling silicon single crystal during crystal growing so as to achieve a flat shape of a solid-liquid interface, that is, to decrease ΔZ in Fig. 5. In this case, however, a rate of cooling of the crystal edge portion should be less than 1.4 times, preferably once, as high as the rate of cooling of the crystal central portion. As described previously, lowering in a rate of cooling of the edge portion leads to poorer efficiency in cooling silicon single crystal. Then, a rate of crystal growing becomes less than 0.9 mm/min and productivity becomes poor. The present invention can achieve less variation in resistivity without lowering productivity in silicon single crystal growing.

By controlling a rate of cooling of the crystal edge portion and a rate of cooling of the crystal central portion so as to set a value for ΔZ in a range from 5 to 15 mm, a rate of change in resistivity in a cross-section perpendicular to central axis during crystal growing L1 can be not higher than 3 % while productivity is maintained. By setting a ratio of a rate of cooling of the crystal edge portion to a rate of cooling of the crystal central portion between 1.4 or higher and 2.0 or lower, a value for ΔZ can be controlled in a range from 5 to 15 mm.

According to the present embodiment, a rate of change in resistivity in a cross-section perpendicular to the central axis of crystal growing can be lowered without using such special facilities as MCZ (Magnetic field applied Czochralski) in which crystal is grown while magnetic field is applied. Therefore, manufacturing cost can be suppressed.

Actual measurement of a rate of change in resistivity

in cross-section A1 perpendicular to central axis during crystal growing L1 of silicon single crystal 2 was attempted in Examples which will be described below.

It is noted that a wafer cut from silicon single crystal obtained in the present invention may be used as it is as a wafer for a power device, or a wafer that has been subjected to high-temperature heat treatment which will be described later may be used.

High-temperature heat treatment is desirably performed in a non-oxidizing atmosphere, because voids or other grown-in defects are not sufficiently eliminated during annealing in an oxidizing atmosphere. The non-oxidizing atmosphere refers to an atmosphere not containing an oxidizing gas such as oxygen, and it includes an inert atmosphere and a reducing atmosphere. The inert atmosphere refers to an atmosphere filled, for example, with such an inert gas as argon, helium, neon, nitrogen, or the like. A reducing atmosphere refers to an atmosphere where such a reducing gas as hydrogen, carbon monoxide, ammonia, or the like is present.

A temperature for heat treatment of a wafer is in a range from 1150 to 1250°C, preferably from 1175 to 1215°C, and further preferably from 1185 to 1200°C.

If a temperature for heat treatment of a silicon substrate is lower than 1150°C, voids or other grown-in defects are not sufficiently eliminated during annealing. Alternatively, if the temperature exceeds 1250°C, a member of a furnace significantly deteriorates.

A time period for heat treatment of a wafer is not shorter than 10 minutes and not longer than 2 hours, preferably not shorter than 30 minutes and not longer than

1.5 hours, and further preferably not shorter than 50 minutes and not longer than 1 hour.

If the time period for heat treatment of a wafer is shorter than 10 minutes, voids or other grown-in defects are not sufficiently eliminated during annealing. Alternatively, if the time period exceeds 2 hours, productivity becomes poor, which is not preferred.

A commercially available heat treatment furnace (or a reaction chamber) for performing heat treatment (annealing) in the manufacturing method according to the present embodiment may be employed, and the furnace is not particularly restricted. It is noted that it is necessary to avoid growth of an oxide film to 2 nm or greater during heat treatment, because attachment of an oxide film to the surface prevents shrinkage and elimination of defects during annealing. Specifically, such measures as decreasing as much as possible an amount of impurity introduced in an atmospheric gas during heat treatment or decreasing as much as possible intake of air from surroundings in inserting a silicon wafer into a furnace are necessary. For example, a noble gas such as argon, in which impurity is suppressed to 5 ppma or lower, is preferred as an atmospheric gas to be used.

A member holding a silicon wafer used in the manufacturing method according to the present embodiment is not particularly restricted, and for example, quartz or the like is employed. These members significantly deteriorate when a temperature for annealing drops excessively. Then, frequent exchange is necessitated, which leads to increase in manufacturing cost.

(Example)

Examples and Comparative Examples of the method of manufacturing silicon single crystal according to the embodiment of the present invention will be described.

Manufacturing of Silicon Single Crystal

An apparatus for manufacturing silicon single crystal with the CZ method was used to grow silicon single crystal (ingot) having a diameter of 200 mm.

Here, the initial silicon melt had boron concentration and phosphorus concentration shown below, and seed crystal was immersed in the initial silicon melt to grow silicon single crystal. A speed of growing of crystal was set to 0.9 mm/min and a rate of cooling of a crystal edge portion was set to 1.9 times as high as a rate of cooling of a crystal central portion.

(1) Example 1

Boron and phosphorus were added to the initial silicon melt, such that boron concentration attained to $1.6\text{E}14$ atoms/cm³ and phosphorus concentration attained to $7.2\text{E}13$ atoms/cm³ (a ratio of phosphorus concentration to boron concentration was 0.45).

(2) Example 2

Boron and phosphorus were added to the initial silicon melt, such that boron concentration attained to $4.0\text{E}14$ atoms/cm³ and phosphorus concentration attained to $1.8\text{E}14$ atoms/cm³ (a ratio of phosphorus concentration to boron concentration was 0.45).

(3) Example 3

Boron and phosphorus were added to the initial silicon melt, such that boron concentration attained to $1.1\text{E}14$ atoms/cm³ and phosphorus concentration attained to

4.6E13 atoms/cm³ (a ratio of phosphorus concentration to boron concentration was 0.42).

(4) Example 4

Boron and phosphorus were added to the initial silicon melt, such that boron concentration attained to 1.6E14 atoms/cm³ and phosphorus concentration attained to 7.5E13 atoms/cm³ (a ratio of phosphorus concentration to boron concentration was 0.47).

(5) Example 5

Boron and phosphorus were added to the initial silicon melt, such that boron concentration attained to 1.6E14 atoms/cm³ and phosphorus concentration attained to 8.0E13 atoms/cm³ (a ratio of phosphorus concentration to boron concentration was 0.50).

(6) Comparative Example 1

Boron was added to the initial silicon melt such that boron concentration attained to 1.0E14 atoms/cm³.

(7) Comparative Example 2

Boron and phosphorus were added to the initial silicon melt, such that boron concentration attained to 1.4E14 atoms/cm³ and phosphorus concentration attained to 4.2E13 atoms/cm³ (a ratio of phosphorus concentration to boron concentration was 0.30).

(8) Comparative Example 3

Boron and phosphorus were added to the initial silicon melt, such that boron concentration attained to 1.8E14 atoms/cm³ and phosphorus concentration attained to 9.9E13 atoms/cm³ (a ratio of phosphorus concentration to boron concentration was 0.55).

Evaluation of Silicon Single Crystal

Grown silicon single crystal was cut perpendicularly to the central axis during crystal growing into slices, to thereby form sliced wafers. Thereafter, the sliced wafers were taken from a plurality of positions along the direction of the central axis during crystal growing, and then mirror finished. The wafers were thus fabricated. The obtained wafers were subjected to high-temperature treatment at 1200°C for 1 hour in an argon gas atmosphere.

Resistivity at each of the center, a point at a radius of 50 mm and a point at a radius of 90 mm of the obtained wafer was measured with a four point probe method.

A result of measurement of resistivity at the central point of each wafer was substituted into Equation (1), to thereby calculate a rate of change in resistivity along the central axis during crystal growing of silicon single crystal.

In addition, a result of measurement of resistivity at each of the center, the point at a radius of 50 mm and the point at a radius of 90 mm of each silicon wafer was substituted into Equation (1), to thereby similarly calculate a radial rate of change in resistivity in a silicon wafer.

Results

(1) Example 1

Table 1 shows the results in Example 1.

Table 1 shows resistivity at the wafer center and a radial rate of change in resistivity in wafer with respect to a solidified fraction at a position where the wafer was taken in silicon single crystal manufactured according to Example 1.

Table 1

Solidified Fraction	Resistivity at Wafer Center [$\Omega\bullet\text{cm}$]	Radial Rate of Change in Resistivity [%]
0.07	140	1.3
0.29	136	0.6
0.51	131	0.4
0.55	130	1.4
0.58	130	1.2
0.61	130	0.9
0.64	130	1.2
0.67	130	0.6
0.71	130	0.5
0.73	132	1.0
0.80	138	0.8

According to Table 1, at a site where the solidified fraction was not higher than 0.80, a minimum value of resistivity along the central axis during crystal growing of silicon single crystal (corresponding to resistivity at the wafer center) was 130 $\Omega\bullet\text{cm}$, the rate of change in resistivity along the central axis during crystal growing was 7.1 %, and a maximum value of the rate of change in resistivity in the cross-section perpendicular to the central axis during crystal growing was 1.4 %.

Namely, manufacturing of silicon single crystal, in which resistivity along the central axis during crystal growing of silicon single crystal was not lower than 50 $\Omega\bullet\text{cm}$, the rate of change in resistivity along the central axis during crystal growing was not higher than 10 %, and

the rate of change in resistivity in the cross-section perpendicular to the central axis during crystal growing was not higher than 3 %, could be realized.

It is noted that the maximum value of the radial rate of change in resistivity at a site where the solidified fraction exceeded 0.80 in the silicon single crystal obtained in the present Example exceeded 3 %.

(2) Comparative Example 1

Table 2 shows results in Comparative Example 1.

Table 2 shows results of resistivity at the silicon wafer center and a radial rate of change in resistivity in a silicon wafer with respect to a solidified fraction at a position where the silicon wafer was taken in silicon single crystal manufactured according to Comparative Example 1.

Table 2

Solidified Fraction	Resistivity at Wafer Center [$\Omega \cdot \text{cm}$]	Radial Rate of Change in Resistivity [%]
0.04	162	4.0
0.17	156	3.5
0.33	148	3.7
0.46	143	2.0
0.62	131	3.2
0.72	122	2.8
0.80	114	3.4

According to Table 2, at a site where the solidified fraction was not higher than 0.80, a minimum value of resistivity along the central axis during crystal growing

of silicon single crystal (corresponding to resistivity at the wafer center) was not lower than 114 $\Omega\cdot\text{cm}$, the rate of change in resistivity along the central axis during crystal growing was 29.6 %, and a maximum value of the rate of change in resistivity in the cross-section perpendicular to the central axis during crystal growing was 4.0 %.

Namely, manufacturing of silicon single crystal, in which resistivity along the central axis during crystal growing of silicon single crystal was not lower than 50 $\Omega\cdot\text{cm}$, the rate of change in resistivity along the central axis during crystal growing was not higher than 10 %, and the rate of change in resistivity in the cross-section perpendicular to the central axis during crystal growing was not higher than 3 %, could not be realized.

(3) Comparison Among Examples and Comparative Examples

Table 3 shows results in Examples 1 to 5 and Comparative Examples 1 to 3.

Table 3 shows results of resistivity at the wafer center in the silicon single crystal manufactured according to each Example and each Comparative Example, the rate of change in resistivity along the central axis during crystal growing, and the rate of change in resistivity in the cross-section perpendicular to the central axis during crystal growing, together with each impurity concentration in the initial silicon melt.

Table 3

	Impurity Concentration in Initial Silicon Melt [atoms/cm ³]			Resistivity at Wafer Center [$\Omega \cdot \text{cm}$]		Rate of Change in Resistivity along Central Axis during Crystal Growing [%]	Rate of Change in Resistivity in Perpendicular Cross-Section [%]
	B	P	P/B Ratio	Maximum Value	Minimum Value		
Example 1	1.6E + 14	7.2E + 13	0.45	140	130	7.1	1.4
Example 2	4.0E + 14	1.8E + 14	0.45	54	50	7.4	1.7
Example 3	1.1E + 14	4.6E + 13	0.42	192	175	8.9	1.5
Example 4	1.6E + 14	7.5E + 13	0.47	136	128	6.1	1.6
Example 5	1.6E + 14	8.0E + 13	0.50	139	132	4.7	2.5
Comparative Example 1	1.0E + 14	0	0.00	163	114	29.8	4.0

Comparative Example 2	1.4E + 14	4.2E + 13	0.30	140	117	16.9	3.4
Comparative Example 3	1.8E + 14	9.9E + 13	0.55	134	124	7.3	3.3

According to Table 3, in Examples 1 to 5, at a site where the solidified fraction was not higher than 0.80, a minimum value of resistivity along the central axis during crystal growing of silicon single crystal ranged from 50 to 175 $\Omega\cdot\text{cm}$, the rate of change in resistivity along the central axis during crystal growing ranged from 4.7 to 8.9 %, and a maximum value of the rate of change in resistivity in the cross-section perpendicular to the central axis during crystal growing ranged from 1.4 to 2.5 %.

Namely, the silicon single crystal obtained in each Example could satisfy such specifications of silicon single crystal required to satisfy specifications of a silicon single crystal wafer for a power device that resistivity along the central axis during crystal growing was not lower than 50 $\Omega\cdot\text{cm}$, the rate of change in resistivity along the central axis during crystal growing was not higher than 10 %, and the rate of change in resistivity in the cross-section perpendicular to the central axis during crystal growing was not higher than 3 %.

In addition, in Examples 1 to 4, at a site where the solidified fraction was not higher than 0.80, a maximum value of the rate of change in resistivity in the cross-section perpendicular to the central axis during crystal growing was not higher than 2 %.

On the other hand, in Comparative Examples 1 to 3, at a site where the solidified fraction was not higher than 0.80, a minimum value of resistivity along the central axis during crystal growing of silicon single crystal ranged from 114 to 124 $\Omega\cdot\text{cm}$, the rate of change in

resistivity along the central axis during crystal growing ranged from 7.3 to 29.8 %, and a maximum value of the rate of change in resistivity in the cross-section perpendicular to the central axis during crystal growing ranged from 3.3 to 4.0 %.

Namely, the silicon single crystal obtained in Comparative Examples could not satisfy specifications of silicon single crystal required to satisfy specifications of a silicon single crystal wafer for power device applications, with regard to the rate of change in resistivity along the central axis during crystal growing and the rate of change in resistivity in the cross-section perpendicular to the central axis during crystal growing.

Attention being paid to relation between the rate of change in resistivity along the central axis during crystal growing and the radial rate of change in resistivity of silicon single crystal fabricated in Examples 1 to 4 and Comparative Examples 1 to 3, such a tendency that the radial rate of change in resistivity is greater as the rate of change in resistivity along the central axis during crystal growing is greater could substantially be confirmed.

According to the measurement results in Examples described above, it was demonstrated that, with the method of manufacturing silicon single crystal according to the present embodiment, that is, by setting boron concentration in the initial silicon melt to 4×10^{14} atoms/cm³ or lower and setting a ratio of phosphorus concentration to boron concentration between 0.42 or higher and 0.50 or lower, p-type silicon single crystal, in which resistivity along the central axis during crystal growing was not

lower than 50 $\Omega\cdot\text{cm}$, the rate of change in resistivity along the central axis during crystal growing was not higher than 10 %, and the rate of change in resistivity in the cross-section perpendicular to the central axis during crystal growing was not higher than 3 % at a site where the solidified fraction was not higher than 0.80, could be manufactured.

In addition, it was demonstrated that, by setting boron concentration in the initial silicon melt to $4\text{E}14$ atoms/ cm^3 or lower and setting a ratio of phosphorus concentration to boron concentration 0.42 or higher and 0.47 or lower, p-type silicon single crystal, in which resistivity along the central axis during crystal growing was not lower than 50 $\Omega\cdot\text{cm}$, the rate of change in resistivity along the central axis during crystal growing was not higher than 10 %, and the rate of change in resistivity in the cross-section perpendicular to the central axis during crystal growing was not higher than 2 % at a site where the solidified fraction was not higher than 0.80, could be manufactured.

The method of manufacturing silicon single crystal, the silicon single crystal, and the wafer according to the embodiment of the present invention have been described above, and the present embodiment achieves the following effect.

P-type silicon single crystal, in which resistivity along the central axis during crystal growing was not lower than 50 $\Omega\cdot\text{cm}$, the rate of change in resistivity along the central axis during crystal growing was not higher than 10 %, and the rate of change in resistivity in the cross-section perpendicular to the central axis during

crystal growing was not higher than 3 %, can be manufactured with the CZ method excellent in mass productivity.

Claims:

1. A method of manufacturing silicon single crystal, characterized in that p-type silicon single crystal is grown with a Czochralski method from an initial silicon melt in which boron concentration is not higher than 4×10^{14} atoms/cm³ and a ratio of phosphorus concentration to boron concentration is not lower than 0.42 and not higher than 0.50.

2. The method of manufacturing silicon single crystal according to claim 1, characterized in that the p-type silicon single crystal is grown by setting a ratio of a rate of cooling of an edge portion of the silicon single crystal to a rate of cooling of a central portion of the silicon single crystal, between 1.4 or higher and 2.0 or lower.

3. P-type silicon single crystal grown with a Czochralski method from an initial silicon melt to which boron and phosphorus were added, characterized in that resistivity along a central axis during crystal growing is not lower than $50 \Omega \cdot \text{cm}$ and a rate of change in resistivity along said central axis during crystal growing is not higher than 10 %.

4. The silicon single crystal according to claim 3, characterized in that a rate of change in resistivity in a cross-section perpendicular to said central axis during crystal growing is not higher than 3 %.

5. A wafer obtained by cutting into a slice, the silicon single crystal according to claim 3 in a manner perpendicular to said central axis during crystal growing.

6. A wafer obtained by cutting into a slice, the silicon single crystal according to claim 4 in a manner perpendicular to said central axis during crystal growing.

7. A wafer having an oxide film after heat treatment not greater than 2 nm, by subjecting the wafer according to claim 5 to heat treatment in a non-oxidizing atmosphere at a temperature not lower than 1150°C and not higher than 1250°C for a time period not shorter than 10 minutes and not longer than 2 hours.

8. The wafer according to claim 7, wherein said non-oxidizing atmosphere is a noble gas atmosphere in which an impurity is not higher than 5 ppma.

9. A wafer having an oxide film after heat treatment not greater than 2 nm, by subjecting the wafer according to claim 6 to heat treatment in a non-oxidizing atmosphere at a temperature not lower than 1150°C and not higher than 1250°C for a time period not shorter than 10 minutes and not longer than 2 hours.

10. The wafer according to claim 9, wherein said non-oxidizing atmosphere is a noble gas atmosphere in which an impurity is not higher than 5 ppma.