

ABSTRACT

A silicon substrate (1) carries an isolating silicon dioxide layer (2) and a relatively weakly and negatively (n) doped monocrystalline silicon wafer (3). A component region (4) is delimited in the wafer by an isolating layer (5). A bipolar transistor (BIP1) in the component region has a positively (p) doped base region (B) which includes a heavily and positively (p^+) doped base connection (B1) and a heavily and negatively (n^+) doped emitter (E1). The transistor (BIP1) has a PN-junction (9) at the underside of the base region (B) and is series-connected with a field effect transistor (JFET1) having a heavily and negatively (n^+) doped drain connection (D1). The component region (4) is weakly doped and the distance from the PN-junction (9) to the silicon dioxide layer (2) is small so that a region (DP1) will be readily depleted of charge carriers when applying voltages (V_E , V_B , V_D) to the transistors (BIP1, JFET1). The voltages produce an electric field (E_D) of low electrical field strength in the depleted region (DP1). This counteracts the breakthrough of a current (I) between the base (B) and the drain connection (D1). The transistors (BIP1, JFET1) withstand high voltages and require only half the space on the substrate (1) required by corresponding earlier known transistors.

Figure 1 for publication together with the Abstract.