Semiconductor device

ABSTRACT OF THE DISCLOSURE

In a vertical transistor comprising a pillar-shaped semiconductor layer and a gate electrode formed to around the pillar-shaped semiconductor layer, it is difficult to form a transistor having a gate length greater than that of the vertical transistor. The present invention provides a semiconductor device which comprises two vertical transistors comprising first and second pillar-shaped semiconductor layers each formed on a first diffusion layer on a substrate. The vertical transistors have a common gate electrode. A first upper diffusion layer formed on a top of the first pillar-shaped semiconductor layer is connected to a source electrode, and a second upper diffusion layer formed on a top of the second pillar-shaped semiconductor layer is connected to a drain electrode. The vertical transistors are connected in series to operate as a composite transistor having a gate length two times greater than that of each of the vertical transistors.

(Figures 1a and 1b)