

(19) World Intellectual Property  
Organization  
International Bureau



(43) International Publication Date  
25 August 2005 (25.08.2005)

PCT

(10) International Publication Number  
**WO 2005/078730 A1**

(51) International Patent Classification<sup>7</sup>: **G11C 11/22**,  
8/18, 16/34

(21) International Application Number:  
PCT/NO2005/000044

(22) International Filing Date: 7 February 2005 (07.02.2005)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:  
2004 0644 13 February 2004 (13.02.2004) NO

(71) Applicant (for all designated States except US): **THIN  
FILM ELECTRONICS ASA** [NO/NO]; P.O. Box 1872  
Vika, N-0124 Oslo (NO).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **KARLSSON,  
Christer** [SE/SE]; Långgatan 81, S-589 55 Linköping

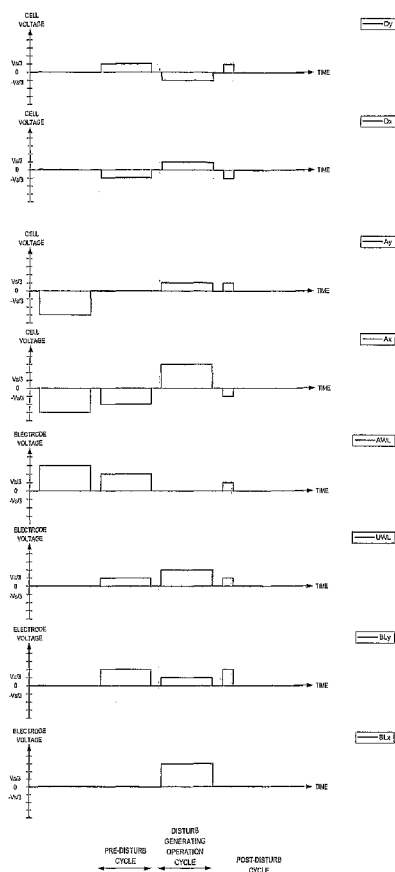
(SE). **HAMBERG, Per** [SE/SE]; Framnäs, S-590 40  
Kisa (SE). **BJÖRKLID, Staffan** [SE/SE]; Syréngatan  
14B, S-582 46 Linköping (SE). **THOMPSON, Michael,  
O.** [US/US]; Cornell University, Bard Hall, Ithaca, NY  
14853-01501 (US). **WOMACK, Richard** [US/US]; 10709  
Santa Monica Avenue, NE, Albuquerque, NM 87122 (US).

(74) Agent: **LEISTAD, Geirr, I.**; Thin Film Electronics ASA,  
P.O. Box 1872 Vika, N-0124 Oslo (NO).

(81) Designated States (unless otherwise indicated, for every  
kind of national protection available): AE, AG, AL, AM,  
AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN,  
CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI,  
GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE,  
KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD,  
MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG,  
PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM,  
TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM,  
ZW.

[Continued on next page]

(54) Title: NON-SWITCHING PRE-AND POST-DISTURB COMPENSATIONAL PULSES



(57) Abstract: In a method for operating a passive matrix-addressable ferroelectric or electret memory device comprising memory cells in the form of a ferroelectric or electret thin-film polarizable memory material exhibiting hysteresis, particularly a ferroelectric or electret polymer thin film, and a first set of parallel electrodes forming word line electrodes in the device and a second set of parallel electrodes forming bit lines in the device, the word lines being oriented orthogonally to the bit lines, such that the word lines and bit lines are in direct contact with the memory cells, which can be set to either of two polarization states or switched between these by applying a switching voltage larger than a coercive voltage of the memory material between a word line and a bit line, a voltage pulse protocol with at least one disturb generating operation cycle is applied for switching selected addressed cells to determined polarization state. The voltage pulse protocol further comprises a pre-disturb and/or post-disturb cycle before and after the disturb generating operation cycle respectively in order to minimize the effect of disturb voltages on non-addressed memory cells, when such voltages are generated thereto in the operation cycle when it is applied for either a write or read operation.



(84) **Designated States** (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

**Published:**

— *with international search report*