

MEMORY DEVICE AND OPERATING METHOD OF THE MEMORY DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

5 **[0001]** The present application claims priority under 35 U.S.C.
§ 119(a) to Korean patent application number 10-2019-0128692,
filed on October 16, 2019, in the Korean Intellectual Property
Office, the entire disclosure of which is incorporated herein by
reference.

BACKGROUND

1. Technical Field

[0002] Various embodiments of the present disclosure
generally relate to an electronic device, and more particularly,
to a memory device and a method operating the memory device.

2. Related Art

[0003] Recently, a paradigm with respect to a computing
environment has changed to ubiquitous computing which is
capable of using a computer system virtually anytime and
anywhere. Accordingly, use of portable electronic devices, such
20 as a mobile phone, a digital camera, and a laptop, has been
rapidly increasing. The portable electronic devices as described
above may generally use memory systems employing memory
devices, that is, data storage devices. A data storage device

may be used as a main memory device or an auxiliary memory device of a portable electronic device.

[0004] A data storage device employing a memory device does not include a mechanical driver, and thus may have
5 excellent stability and durability with an extremely high information access speed and low power consumption. Examples of a memory system having the above-stated characteristics are a data storage device including a Universal Serial Bus (USB) memory device, a memory card having various interfaces, and a
10 Solid-State Drive (SSD).

[0005] Memory devices are generally classified into volatile memory devices and nonvolatile memory devices.

[0006] A nonvolatile memory device may have comparatively low write and read speeds, but may retain stored data in the
15 absence of supplied power. Therefore, a nonvolatile memory device may be used when there is a need for storing data which should be retained regardless of a supply of power. Examples of nonvolatile memory devices include Read Only Memory (ROM), Mask ROM (MROM), Programmable ROM (PROM), Erasable
20 Programmable ROM (EPROM), Electrically Erasable Programmable ROM (EEPROM), flash memory, Phase change Random Access Memory (PRAM), Magnetic RAM (MRAM), Resistive RAM (RRAM), and Ferroelectric RAM (FRAM). Flash memory may be classified into NOR-type memory and NAND-type memory.

SUMMARY

[0007] According to an embodiment, a memory device may include a memory cell array including memory cells that are
5 programmed into a plurality of program states, a peripheral circuit configured to perform a read operation on the memory cell array, and control logic configured to control the peripheral circuit to perform the read operation and to control the peripheral circuits to perform a masking process on first memory
10 cells having a threshold voltage level higher than a first read level and second memory cells having a threshold voltage level lower than a second read level among the memory cells during the read operation.

[0008] According to an embodiment, a memory device may
15 include a page including a plurality of memory cells coupled in common to a word line, a peripheral circuit configured to perform a read operation on the page, and control logic configured to control the peripheral circuit to perform the read operation, wherein, during the read operation, the control logic
20 controls the peripheral circuits to perform a first sensing operation in which first memory cells having a threshold voltage level higher than or equal to a first read level that is higher than a main read level, among the plurality of memory cells, are sensed, a second sensing operation in which second memory

cells having a threshold voltage level lower than or equal to a second read level that is lower than the main read level, among the plurality of memory cells, are sensed, and a third sensing operation in which the plurality of memory cells are sensed in a state where a masking process is performed on the first memory cells and the second memory cells.

[0009] According to an embodiment, a method of operating a memory device may include performing a first sensing operation in which first memory cells having a threshold voltage level higher than or equal to a first read level that is higher than a main read level, among a plurality of memory cells, are sensed, performing a second sensing operation in which second memory cells having a threshold voltage level lower than or equal to a second read level that is lower than the main read level, among the plurality of memory cells, are sensed, performing a masking process on the first memory cells and the second memory cells, and performing a third sensing operation in which whether a threshold voltage level of the plurality of memory cells is higher or lower than the main read level is sensed.

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BRIEF DESCRIPTION OF THE DRAWINGS

[0010] FIG. 1 is a block diagram illustrating a memory system according to an embodiment;

[0011] FIG. 2 is a diagram illustrating a memory device

shown in FIG. 1;

[0012] FIG. 3 is a diagram illustrating a memory block shown in FIG. 2;

[0013] FIG. 4 is a diagram illustrating an embodiment of a
5 three-dimensionally structured memory block;

[0014] FIG. 5 is a diagram illustrating a page buffer shown in FIG. 2;

[0015] FIG. 6 is a diagram illustrating a threshold voltage distribution of memory cells;

10 **[0016]** FIG. 7 is a flowchart illustrating a method of operating a memory device according to an embodiment;

[0017] FIGs. 8, 9 and 10 are distribution charts of a threshold voltage illustrating a method of operating a memory device according to an embodiment;

15 **[0018]** FIG. 11 is a waveform diagram of signals illustrating an operation of a page buffer according to an embodiment;

[0019] FIG. 12 is a waveform diagram of signals illustrating an operation of a page buffer according to another embodiment;

[0020] FIG. 13 is a waveform diagram of signals illustrating
20 an operation of a page buffer according to another embodiment;

[0021] FIG. 14 is a diagram illustrating another embodiment of a memory system;

[0022] FIG. 15 is a diagram illustrating another embodiment of a memory system;

[0023] FIG. 16 is a diagram illustrating another embodiment of a memory system; and

[0024] FIG. 17 is a diagram illustrating another embodiment of a memory system.

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DETAILED DESCRIPTION

[0025] Hereinafter, specific structural or functional descriptions of examples of embodiments in accordance with concepts which are disclosed in this specification are illustrated only to describe the examples of embodiments in accordance with the concepts and the examples of embodiments in accordance with the concepts may be carried out by various forms but the descriptions are not limited to the examples of embodiments described in this specification.

10 **[0026]** Hereinafter, embodiments of the present disclosure are described with reference to the accompanying drawings in order for those skilled in the art to be able to readily implement the technical spirit of the present disclosure.

[0027] Various embodiments are directed to a memory device capable of improving the reliability of a read operation, and a method of operating the memory device.

[0028] FIG. 1 is a diagram illustrating a memory system 1000 according to an embodiment.

[0029] Referring to FIG. 1, the memory system 1000 may

include a memory device 1100 storing data and a memory controller 1200 controlling the memory device 1100 in response to control of a host 2000.

[0030] The host 2000 may communicate with the memory system 1000 using an interface protocol such as Peripheral Component Interconnect-Express (PCI-E), Advanced Technology Attachment (ATA), Serial ATA (SATA), Parallel ATA (PATA), or serial attached SCSI (SAS). In addition, the interface protocols provided for the purpose of communication between the host 2000 and the memory system 1000 are not limited to the above examples and may be one of interface protocols such as a Universal Serial Bus (USB), a Multi-Media Card (MMC), an Enhanced Small Disk Interface (ESDI), or Integrated Drive Electronics (IDE).

[0031] The memory controller 1200 may control the general operations of the memory system 1000 and control data exchange between the host 2000 and the memory device 1100. For example, the memory controller 1200 may control the memory device 1100 to program or read data in response to a request from the host 2000. During a program operation, the memory controller 1200 may transmit a command CMD, an address ADD, and data DATA to be programmed corresponding to the program operation to the memory device 1100. In addition, during a read operation, the memory controller 1200

may receive and temporarily store the data DATA read from the memory device 1100 and may transmit the temporarily stored data DATA to the host 2000.

[0032] The memory device 1100 may perform a program operation, a read operation, or an erase operation under the control of the memory controller 1200. According to an embodiment, the memory device 1100 may include Double Data Rate Synchronous Dynamic Random Access Memory (DDR SDRAM), Low Power Double Data Rate4 (LPDDR4) SDRAM, Graphics Double Data Rate (GDDR) SDRAM, Low Power DDR (LPDDR), Rambus Dynamic Random Access Memory (RDRAM), or flash memory.

[0033] FIG. 2 is a diagram illustrating the memory device 1100 shown in FIG. 1.

[0034] Referring to FIG. 2, the memory device 1100 may include a memory cell array 100 storing data. The memory device 1100 may include a peripheral circuit 200 configured to perform a program operation to store data in the memory cell array 100, a read operation to output the stored data, and an erase operation to erase the stored data. The memory device 1100 may include control logic 300 which controls the peripheral circuit 200 in response to control of the memory controller 1200 shown in FIG 1. The control logic 300 may be implemented as hardware, software, or a combination of hardware and software.

For example, the control logic 300 may be a control logic circuit operating in accordance with an algorithm and/or a processor executing control logic code.

[0035] The memory cell array 100 may include a plurality of
5 memory blocks (MB1 to MBk) 110, where k is a positive integer. Local lines LL and bit lines BL1 to BLm may be coupled to each of the memory blocks (MB1 to MBk) 110, where m is a positive integer. For example, the local lines LL may include a first select line, a second select line, and a plurality of word lines
10 arranged between the first and second select lines. In addition, the local lines LL may include dummy lines arranged between the first select line and the word lines and between the second select line and the word lines. The first select line may be a source select line and the second select line may be a drain
15 select line. For example, the local lines LL may include word lines, drain and source select lines, and source lines SL. For example, the local lines LL may further include dummy lines. For example, the local lines LL may further include pipe lines. The local lines LL may be coupled to the memory blocks (MB1 to
20 MBk) 110, respectively, and the bit lines BL1 to BLm may be commonly coupled to the memory blocks (MB1 to MBk) 110. The memory blocks (MB1 to MBk) 110 may have a two-dimensional or three-dimensional structure. For example, in the two-dimensionally structured memory blocks 110, memory cells may

be arranged in parallel with a substrate. For example, in the three-dimensionally structured memory blocks 110, memory cells may be stacked in a vertical direction to the substrate.

[0036] The peripheral circuit 200 may be configured to perform program, read, and erase operations on the selected memory block 110 in response to control of the control logic 300. For example, the peripheral circuit 200 may include a voltage generating circuit 210, a row decoder 220, a page buffer group 230, a column decoder 240, an input/output circuit 250, a pass/fail check circuit 260, and a source line driver 270.

[0037] The voltage generating circuit 210 may generate various operating voltages V_{op} applied to perform program, read and erase operations in response to an operation signal OP_CMD . In addition, the voltage generating circuit 210 may selectively discharge the local lines LL in response to the operation signal OP_CMD . For example, the voltage generating circuit 210 may generate a read voltage, a program voltage, a pass voltage, and the like in response to control of the control logic 300.

[0038] The row decoder 220 may transmit the operating voltages V_{op} to the local lines LL coupled to the selected memory block 110 in response to row decoder control signals $AD_signals$. For example, the row decoder 220 may apply a read voltage generated by the voltage generating circuit 210 to a selected word line, among the local lines LL , and may apply a

pass voltage generated by the voltage generating circuit 210 to unselected word lines in response to the row decoder control signals AD_signals during a read operation. In addition, the row decoder 220 may apply a program voltage generated by the voltage generating circuit 210 to a selected word line, among the local lines LL, and may apply a pass voltage generated by the voltage generating circuit 210 to unselected word lines in response to the row decoder control signals AD_signals during a program operation.

[0039] The page buffer group 230 may include a plurality of page buffers PB1 to PBm coupled to the bit lines BL1 to BLm, respectively. The page buffers PB1 to PBm may operate in response to page buffer control signals PBSIGNALS. For example, the page buffers PB1 to PBm may temporarily store data to be programmed and adjust a potential level of the bit lines BL1 to BLm based on the temporarily stored data to be programmed during a program operation. In addition, a voltage or a current of the bit lines BL1 to BLm may be sensed to read data during a read or verify operation.

[0040] The column decoder 240 may transmit data between the input/output circuit 250 and the page buffer group 230 in response to a column address CADD. For example, the column decoder 240 may exchange data with the page buffers PB1 to PBm through data lines DL, or exchange data with the

input/output circuit 250 through column lines CL.

[0041] The input/output circuit 250 may transmit the command CMD and the address ADD received from the memory controller 1200 shown in FIG. 1 to the control logic 300, or may
5 exchange the data DATA with the column decoder 240.

[0042] The pass/fail check circuit 260 may generate a reference current in response to an allowable bit VRY_BIT<#> and output a pass signal PASS or a fail signal FAIL by comparing a sensing voltage VPB received from the page buffer group 230
10 with a reference voltage generated by the reference current during a read operation or a program verify operation. The sensing voltage VPB may be a voltage controlled based on the number of memory cells that are determined as passed during a program verify operation.

[0043] The source line driver 270 may be coupled to the memory cells included in the memory cell array 100 through the source line SL and may control a voltage applied to the source line SL. The source line driver 270 may receive a source line control signal CTRL_SL from the control logic 300 and control a
15 source line voltage applied to the source line SL based on the source line control signal CTRL_SL.
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[0044] The control logic 300 may control the peripheral circuit 200 by outputting the operation signal OP_CMD, the row decoder control signals AD_signals, the page buffer control

signals PBSIGNALS, and the allowable bit VRY_BIT<#> in response to the command CMD and the address ADD.

[0045] The control logic 300 may control the peripheral circuit 200 to perform a first sensing operation on a first read level higher than a main read level, a second sensing operation on a second read level lower than the main read level, and a main sensing operation on the main read level during a read operation. The control logic 300 may control the page buffer group 230 to apply a ground voltage to bit lines of memory cells having a threshold voltage level higher than the first read level and memory cells having a threshold voltage level lower than the second read level based on results of the first sensing operation and the second sensing operation, during the main sensing operation.

[0046] Accordingly, sensing error caused by a noise phenomenon between bit lines may be reduced by performing a masking process on the memory cells having a threshold voltage level higher than the first read level and the memory cells having a threshold voltage level lower than the second read level during the read operation on the memory cells having a threshold voltage distribution between the first read level and the second read level. In other words, a probability that the ground voltage is applied to bit lines adjacent to the bit lines coupled to the memory cells having the threshold voltage

distribution between the first read level and the second read level may be high. Therefore, the noise phenomenon of the bit lines coupled to the memory cells having the threshold voltage distribution between the first read level and the second read level may be prevented or lessened.

[0047] FIG. 3 is a diagram illustrating the memory block 110 shown in FIG. 2.

[0048] Referring to FIG. 3, the memory block 110 may be configured such that a plurality of word lines arranged in parallel with each other may be coupled between a first select line and a second select line. The first select line may be a source select line SSL and the second select line may be a drain select line DSL. For example, the memory block 110 may include a plurality of strings ST coupled between the bit lines BL1 to BLm and the source line SL. The bit lines BL1 to BLm may be coupled to the strings ST, respectively, and the source line SL may be commonly coupled to the strings ST. Because the strings ST may have the same configuration, the string ST coupled to the first bit line BL1 is described as an example.

[0049] The string ST may include a source select transistor SST, a plurality of memory cells F1 to F16, and a drain select transistor DST coupled in series between the source line SL and the first bit line BL1. The single string ST may include at least one source select transistor SST and at least one drain select

transistor DST, and may include more memory cells than the memory cells F1 to F16 shown in FIG. 3.

[0050] A source of the source select transistor SST may be coupled to the source line SL, and a drain of the drain select transistor DST may be coupled to the first bit line BL1. The memory cells F1 to F16 may be coupled in series between the source select transistor SST and the drain select transistor DST. Gates of the source select transistors SST included in different strings ST may be coupled to the source select line SSL, gates of the drain select transistors DST may be coupled to the drain select line DSL, and gates of the memory cells F1 to F16 may be coupled to a plurality of word lines WL1 to WL16, respectively. A group of memory cells coupled to the same word line, among memory cells included in the different strings ST, may be referred to as a page PPG. Therefore, the memory block 110 may include as many pages PPG as the number of word lines WL1 to WL16.

[0051] FIG. 4 is a diagram illustrating an embodiment of the three-dimensionally structured memory block 110.

[0052] Referring to FIG. 4, the memory cell array 100 may include the plurality of memory blocks (MB1 to MBk) 110. The memory block 110 may include a plurality of strings ST11 to ST1m and ST21 to ST2m. According to an embodiment, each of the plurality of strings ST11 to ST1m and ST21 to ST2m may

have an 'I' shape or a 'U' shape. In the first memory block MB1, m strings may be arranged in a row direction (X direction). For convenience of explanation, FIG. 4 illustrates two strings arranged in a column direction (Y direction). However, three or
5 more strings may be arranged in the column direction (Y direction).

[0053] Each of the plurality of strings ST11 to ST1m and ST21 to ST2m may include at least one source select transistor SST, first to nth memory cells MC1 to MCn, and at least one
10 drain select transistor DST.

[0054] The source select transistor SST of each string may be coupled between the source line SL and the memory cells MC1 to MCn. Source select transistors of strings arranged in the same row may be coupled to the same source select line. Source
15 select transistors of the strings ST11 to ST1m arranged in the first row may be coupled to a first source select line SSL1. Source select transistors of the strings ST21 to ST2m arranged in the second row may be coupled to a second source select line SSL2. According to another embodiment, source select
20 transistors of the strings ST11 to ST1m and ST21 to ST2m may be coupled in common to a single source select line.

[0055] The first to nth memory cells MC1 to MCn of each string may be coupled in series between the source select transistor SST and the drain select transistor DST. Gates of the

first to nth memory cells MC1 to MCn may be coupled to the first to nth word lines WL1 to WLn, respectively.

[0056] According to an embodiment, at least one of the first to nth memory cells MC1 to MCn may serve as a dummy memory cell. When a dummy memory cell is provided, a voltage or current of the corresponding string may be stably controlled. Accordingly, the reliability of data stored in the memory block 110 may be improved.

[0057] The drain select transistor DST of each string may be coupled between the bit line and the memory cells MC1 to MCn. The drain select transistors DST of the strings arranged in the row direction may be coupled to a drain select line extending in the row direction. The drain select transistors DST of the strings ST11 to ST1m in the first row may be coupled to a first drain select line DSL1. The drain select transistors DST of the strings ST21 to ST2m in the second row may be coupled to a second drain select line DSL2.

[0058] FIG. 5 is a diagram illustrating the page buffer shown in FIG. 2.

[0059] Because the plurality of page buffers PB1 to PBm may be configured in similar manners, one of the page buffers (PB1) is described as an example.

[0060] Referring to FIG. 5, the page buffer PB1 may include a bit line coupling circuit 231, a bit line set-up circuit 232, a page

buffer sensing circuit 233, a sensing node coupling circuit 234, a current control circuit 235, a sensing node precharge circuit 236, a main latch 237, a first discharge circuit 238, a sub-latch 239, and a second discharge circuit 241.

5 **[0061]** The bit line coupling circuit 231 may be coupled between the bit line BL1 and a bit line coupling node BLCM and may include an NMOS transistor N1 operating in response to a bit line select signal PB_SELBL. The NMOS transistor N1 may be turned on or off in response to the bit line select signal
10 PB_SELBL.

[0062] The bit line set-up circuit 232 may be coupled between a power voltage VEXT terminal, ground power Vss, and the bit line coupling node BLCM, and may include an NMOS transistor N2 operating in response to a bit line discharge signal
15 BLDIS, and a PMOS transistor P1 operating in response to a bit line precharge signal BLPRE_N. The NMOS transistor N2 may be turned on or off in response to the bit line discharge signal BLDIS and may apply the ground power Vss to the bit line coupling node BLCM. The PMOS transistor P1 may apply the
20 power voltage VEXT to the bit line coupling node BLCM in response to the bit line precharge signal BLPRE_N.

[0063] The page buffer sensing circuit 233 may be coupled between the bit line coupling node BLCM and a current sensing node CSO and may include an NMOS transistor N3 operating in

response to a page buffer sensing signal PB_SENSE. The NMOS transistor N3 may be turned on or off in response to the page buffer sensing signal PB_SENSE.

[0064] The sensing node coupling circuit 234 may be coupled
5 between the current sensing node CSO and a sensing node SO and may include an NMOS transistor N4 operating in response to a node coupling signal TRANSO. The NMOS transistor N4 may be turned on or off in response to the node coupling signal TRANSO.

[0065] The current control circuit 235 may include a clamp
10 circuit 235A and a sensing discharge circuit 235B.

[0066] The clamp circuit 235A may include an NMOS transistor N5 and PMOS transistors P2 and P3. The PMOS transistor P2 may be coupled between a core voltage VCORE terminal and a sense amplifier node SAN and may be turned on
15 or off in response to a potential of a second sub-node QS of the sub-latch 239. The PMOS transistor P3 may be coupled between the sense amplifier node SAN and the current sensing node CSO and may be turned on or off in response to an internal sensing node precharge signal SA_PRECH_N. The NMOS transistor N5
20 may be coupled between the sense amplifier node SAN and the current sensing node CSO and may apply a sensing current for sensing the bit line BL1 to the current sensing node CSO in response to a current sensing signal SA_CSOC.

[0067] The sensing discharge circuit 235B may be coupled

between the current sensing node CSO and a node QN of the first discharge circuit 238 and may include an NMOS transistor N8 operating in response to an internal sensing node discharge signal SA_DISCH. The NMOS transistor N8 may be turned on or
5 off in response to the internal sensing node discharge signal SA_DISCH.

[0068] The sensing node precharge circuit 236 may be coupled between the core voltage VCORE terminal and the sensing node SO and may include a PMOS transistor P5
10 operating in response to a precharge signal PRECHSO_N. The PMOS transistor P5 may supply the core voltage VCORE to the sensing node SO in response to the precharge signal PRECHSO_N.

[0069] The main latch 237 may include an NMOS transistor N7, an NMOS transistor N9, a latch LATM, and a main latch
15 reset/setup circuit RSEM. The main latch 237 may temporarily store data sensed during a read operation.

[0070] The latch LATM may include inverters IV1 and IV2. The inverters IV1 and IV2 may be coupled in anti-parallel with each other between first and second main nodes QM_N and QM
20 of the latch LATM. An input terminal of the inverter IV1 may be coupled to the second main node QM and an output terminal of the inverter IV1 may be coupled to the first main node QM_N. An input terminal of the inverter IV2 may be coupled to the first main node QM_N and an output terminal of the inverter IV2 may

be coupled to the second main node QM.

[0071] The NMOS transistor N9 and the NMOS transistor N7 may be coupled in series between the sensing node SO and the ground power Vss and may apply or block the ground power Vss to the sensing node SO in response to a main data transmission signal TRANM and a potential of the first main node QM_N. The NMOS transistor N9 may be turned on or off in response to the main data transmission signal TRANM, and the NMOS transistor N7 may be turned on or off in response to a potential of the first main node QM_N.

[0072] The main latch reset/setup circuit RSEM may be coupled to the first and second main nodes QM_N and QM of the latch LATM and may reset or set up the latch LATM. The main latch reset/setup circuit RSEM may include NMOS transistors N10 and N11. The NMOS transistor N10 may couple the second main node QM of the latch LATM to the common node COM in response to a main reset signal MRST. The NMOS transistor N11 may couple the first main node QM_N of the latch LATM to the common node COM in response to a main setup signal MSET.

The main latch reset/setup circuit RSEM may couple the common node COM to the second main node QM in response to the main reset signal MRST to initialize the latch LATM such that the second main node QM reaches a low level during an initialization operation of the latch LATM and may control the first main node

QM_N to reach a low level or a high level according to a potential of the common node COM which is determined according to a sensed data value in response to the main setup signal MSET during a sensing operation of the latch LATM.

5 **[0073]** The first discharge circuit 238 may include NMOS transistors N12 and N13 coupled in series between the sensing node SO and the ground power Vss. The NMOS transistor N12 may be turned on or off in response to a transmission signal TRANS and the NMOS transistor N13 may be turned on or off in
10 response to a potential of a second sub-node QS of the sub-latch 239.

[0074] The sub-latch 239 may include a latch LATS and a sub-latch reset/setup circuit RSES.

[0075] The latch LATS may include inverters IV3 and IV4.
15 The inverters IV3 and IV4 may be coupled in anti-parallel with each other between a first sub-node QS_N and the second sub-node QS of the latch LATS. For example, an input terminal of the inverter IV3 may be coupled to the second sub-node QS and an output terminal of the inverter IV3 may be coupled to the
20 first sub-node QS_N. An input terminal of the inverter IV4 may be coupled to the first sub-node QS_N and an output terminal of the inverter IV4 may be coupled to the second sub-node QS.

[0076] The sub-latch reset/setup circuit RSES may be coupled to the first sub-node QS_N and the second sub-node QS and

may reset or set up the latch LATS. The sub-latch reset/setup circuit RSES may include NMOS transistors N14, N15 and N16. The NMOS transistor N14 may couple the second sub-node QS of the latch LATS to the common node COM in response to a sub-
5 reset signal SRST. The NMOS transistor N15 may couple the first sub-node QS_N of the latch LATS to the common node COM in response to a sub-setup signal SSET. When a reset operation or a setup operation of the latch LATS is performed, the ground power Vss may be coupled to the common node COM. The NMOS
10 transistor N16 may be coupled between the first sub-node QS_N and a terminal of the ground power Vss and may be turned on in response to a reset signal PBRST.

[0077] The second discharge circuit 241 may include a NMOS transistor N17 that is coupled between the common node COM
15 and a terminal of the ground power Vss and is turned on or off in response to a potential of the sensing node SO.

[0078] FIG. 6 is a diagram illustrating a threshold voltage distribution of memory cells.

[0079] Referring to FIG. 6, a plurality of memory cells
20 included in the single page PPG of FIG. 3 may have a threshold voltage distribution corresponding to a plurality of program states when a program operation is performed.

[0080] For example, when the plurality of memory cells are programmed by a Triple Level Cell (TLC) method, the plurality of

memory cells may have a threshold voltage distribution corresponding to an erase state P0 and first to seventh program states P1 to P7. The memory cells programmed by the TLC method may sense a corresponding program state by using a plurality of read voltages R1 to R7 during a read operation. For example, when a threshold voltage of a target memory cell is greater than the third read voltage R3 according to a result of a read operation using the third read voltage R3, and when the threshold voltage V_t of the target memory cell is smaller than the fourth read voltage R4 according to a result of a read operation using the fourth read voltage R4, it is sensed that the target memory cell corresponds to the third program state, therefore, data corresponding to the third program state may be read.

[0081] FIG. 7 is a flowchart illustrating a method of operating a memory device according to an embodiment.

[0082] FIGs. 8 to 10 are distribution charts of a threshold voltage illustrating a method of operating a memory device according to an embodiment.

[0083] A method of performing a read operation of a memory device according to an embodiment is described below with reference to FIGs. 2 and 7 to 10.

[0084] In an embodiment, a read operation using the fourth read voltage R4 among the read operations using the read

voltage is described as an example. In this example, the fourth read voltage R4 may be, for example, a main read level.

[0085] During the read operation, the control logic 300 of the memory device may control the peripheral circuit 200 to perform
5 a sensing operation pertaining to a first read level R4_1 higher than a level of the fourth read voltage R4 to sense memory cells corresponding to a region A as shown in FIG. 8 (S710). A sensing result may be stored in the page buffers PB1 to PBm of the page buffer group 230.

10 **[0086]** In other words, the memory cells having a threshold voltage that have a level that is higher than or equal to the first read level R4_1 higher than the level of the fourth read voltage R4, i.e., a main read level, may be sensed. In an embodiment, the region A may correspond to the memory cells having a
15 threshold voltage that have a level that is higher than or equal to the first read level R4_1 higher than the level of the fourth read voltage R4.

[0087] The control logic 300 of the memory device may control the peripheral circuit 200 to perform a sensing operation
20 pertaining to a second read level R4_2 lower than the level of the fourth read voltage R4 to sense memory cells corresponding to a region B as shown in FIG. 9 (S720). A sensing result may be stored in the page buffers PB1 to PBm of the page buffer group 230.

[0088] In other words, the memory cells having a threshold voltage that have a level that is lower than or equal to the second read level R4_2 lower than the level of the fourth read voltage R4, i.e., the main read level, may be sensed. In an
5 embodiment, the region B may correspond to the memory cells having a threshold voltage that have a level that is lower than or equal to the second read level R4_2 lower than the level of the fourth read voltage R4.

[0089] According to an embodiment, it is described that step
10 S720 is performed after step S710 is performed. Alternatively, however, step S710 may be performed after step S720 is performed.

[0090] A masking process may be performed on the memory cells corresponding to the region A and the region B, which are
15 sensed according to the sensing results of step S710 and step S720, respectively (S730). The masking process may control bit lines coupled to the memory cells corresponding to the region A and the region B to have a ground level during a sensing operation pertaining to the main read level subsequent to the
20 masking process.

[0091] The page buffers PB1 to PBm of the page buffer group
230 may control the bit lines, which are coupled to the memory cells corresponding to the region A and the region B, to have the ground level during the sensing operation pertaining to the main

read level according to the sensing results of step S710 and step S720.

[0092] Subsequently, a sensing operation pertaining to the main read level may be performed to perform a read operation of memory cells corresponding to a region C (S740). In other words, among the memory cells corresponding to the region C, memory cells having a threshold voltage greater than or equal to the fourth read voltage R4, i.e., the main read level, and memory cells having a threshold voltage smaller than or equal to the fourth read voltage R4 may be sensed and a sensing result may be stored in the page buffer group 230. Referring to FIG. 10, a sensing operation pertaining to the main read level may be performed with respect to the memory cells corresponding to the region C, other than the memory cells corresponding to the region A and having the threshold voltage level which is higher than or equal to the first read level R4_1 and the memory cells corresponding to the region B and having the threshold voltage level which is lower than or equal to the second read level R4_2.

[0093] The page buffer group 230 may temporarily store read data based on the result of the sensing operation pertaining to the first read level and the second read level and the result of the sensing operation pertaining to the main read level and may output the temporarily stored read data.

[0094] Because the bit lines coupled to the memory cells

corresponding to the region A or the region B have a ground level by the page buffer group 230 during the sensing operation pertaining to the main read level, a probability that bit lines adjacent to bit lines coupled to the memory cells corresponding to the region C, during the sensing operation pertaining to the memory cells corresponding to the region C, have a ground level may be high. Accordingly, noise caused by a bit line coupling phenomenon may be prevented or lessened during the sensing operation pertaining to the main read level.

10 **[0095]** FIG. 11 is a waveform diagram of signals illustrating an operation of a page buffer according to an embodiment.

[0096] An operation of a page buffer according to an embodiment is described below with reference to FIGs. 5 and 8 to 11. When a read operation is performed, a plurality of page buffers operate in a similar manner. Accordingly, the page buffer PB1 is described as an example.

[0097] In an embodiment, a read operation using the fourth read voltage R4 among the read operations using a plurality of read voltages is described as an example.

20 **[0098]** The page buffer PB1 may perform an initialization operation during a period t1. For example, the PMOS transistor P5 may be turned on in response to the precharge signal PRECHSO_N to apply the core voltage V_{CORE} to the sensing node SO. Accordingly, the NMOS transistor N17 of the second

discharge circuit 241 may be turned on to apply the ground power V_{ss} to the common node COM. Subsequently, the main reset signal MRST having a high level may be applied to the main latch reset/setup circuit RSEM to initialize the second main node QM of the latch LATM to a low level. In addition, the sub-
5 reset signal SRST having a high level may be applied to the sub-latch reset/setup circuit RSES to initialize the second sub-node QS of the latch LATS to a low level.

[0099] The first read level voltage R4_1 may be applied to
10 the word line WL corresponding to a selected page during a period t_2 . The first read level voltage R4_1 may correspond to the first read level R4_1 shown in FIG. 8.

[00100] The PMOS transistor P2 of the clamp circuit 235A may be turned on in response to a potential of the second sub-node
15 QS, and the PMOS transistor P3 of the clamp circuit 235A may be turned on in response to the internal sensing node precharge signal SA_PRECH_N to apply the core voltage V_{CORE} to the current sensing node CSO. The NMOS transistor N1 of the bit line coupling circuit 231 may be turned on in response to the bit
20 line select signal PB_SELBL and the NMOS transistor N3 of the page buffer sensing circuit 233 may be turned on in response to the page buffer sensing signal PB_SENSE to electrically couple the bit line BL1 to the current sensing node CSO to which the core voltage V_{CORE} is applied. Accordingly, the bit line BL1 may

be precharged to a predetermined level. The word “predetermined” as used herein with respect to a parameter, such as a predetermined level, means that a value for the parameter is determined prior to the parameter being used in a process or algorithm. For some embodiments, the value for the parameter is determined before the process or algorithm begins. In other embodiments, the value for the parameter is determined during the process or algorithm but before the parameter is used in the process or algorithm.

10 **[00101]** The PMOS transistor P3 may be turned off in response to the internal sensing node precharge signal SA_PRECH_N during a period t3. Accordingly, a cell current of the bit line BL1 may vary according to a threshold voltage of a memory cell coupled to the bit line BL1. The NMOS transistor N4 may maintain a turn-on state during a sensing time Sensing time of the period t3 and may then be turned off in response to the node coupling signal TRANSO. Accordingly, a potential level of the sensing node SO may be maintained at a high level or may be discharged to a low level according to a cell current of the bit line BL1. Subsequently, the main setup signal MSET having a high level may be applied to the main latch reset/setup circuit RSEM, such that the first main node QM_N of the latch LATM maintains a high level or is set up to have a low level. In other words, when a threshold voltage of a memory cell coupled to the

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bit line BL1 is greater than the first read level voltage R4_1, the first main node QM_N may be set up to have a low level, and when the threshold voltage of the memory cell coupled to the bit line BL1 is smaller than the first read level voltage R4_1, the first main node QM_N may maintain a high level.

[00102] The second read level voltage R4_2 may be applied to the word line WL corresponding to the selected page during a period t4. The second read level voltage R4_2 may correspond to the second read level R4_2 shown in FIG. 9.

[00103] The PMOS transistor P2 of the clamp circuit 235A may be turned on in response to a potential of the second sub-node QS, and the PMOS transistor P3 of the clamp circuit 235A may be turned on in response to the internal sensing node precharge signal SA_PRECH_N to apply the core voltage VCORE to the current sensing node CSO. The NMOS transistor N1 of the bit line coupling circuit 231 may be turned on in response to the bit line select signal PB_SELBL and the NMOS transistor N3 of the page buffer sensing circuit 233 may be turned on in response to the page buffer sensing signal PB_SENSE to electrically couple the bit line BL1 to the current sensing node CSO to which the core voltage VCORE is applied. Accordingly, the bit line BL1 may be precharged to a predetermined level.

[00104] The PMOS transistor P3 may be turned off in response to the internal sensing node precharge signal SA_PRECH_N

during a period t_5 . Accordingly, a cell current of the bit line BL1 may vary according to a threshold voltage of a memory cell coupled to the bit line BL1. The NMOS transistor N4 may maintain a turn-on state during the sensing time Sensing time of
5 the period t_5 and may then be turned off in response to the node coupling signal TRANSO. Accordingly, a potential level of the sensing node SO may be maintained at a high level or may be discharged to a low level according to the cell current of the bit line BL1. The reset signal PBRST having a high level may be
10 applied to the sub-latch reset/setup circuit RSES to set the first sub-node QS_N of the latch LATS to a low level. Subsequently, the sub-reset signal SRST having a high level may be applied to the sub-latch reset/setup circuit RSES, such that the second sub-node QS of the latch LATS maintains a high level or is set up
15 to have a low level. In other words, when a threshold voltage of a memory cell coupled to the bit line BL1 is greater than the second read level voltage R4_2, the second sub-node QS may be set up to have a low level, and when the threshold voltage of the memory cell coupled to the bit line BL1 is smaller than the
20 second read level voltage R4_2, the second sub-node QS may maintain a high level.

[00105] Sensing data stored in the latch LATM may be transmitted to the latch LATS during a period t_6 . Accordingly, data based on the sensing data that is sensed during the period

t5 and the sensing data that is sensed during the period t3 may be newly stored in the latch LATS. For example, the PMOS transistor P5 may be turned on in response to the precharge signal PRECHSO_N to apply the power voltage VEXT to the sensing node SO. Accordingly, the sensing node SO may be precharged to a predetermined level. Subsequently, when the NMOS transistor N9 is turned on in response to the main data transmission signal TRANM, a potential level of the sensing node SO may be maintained at the precharged level or may be discharged to a low level according to a potential level of the first main node QM_N. Subsequently, the sub-setup signal SSET having a high level may be applied to the sub-latch reset/setup circuit RSES, such that the second sub-node QS of the latch LATS maintains a previous level or is set up to have a high level.

15 **[00106]** For example, when a level of a threshold voltage of a memory cell is higher than the first read level R4_1, sensing data stored in the latch LATM may be transmitted to the latch LATS and the second sub-node QS of the latch LATS may be set to have a high level. In addition, when the level of the

20 threshold voltage of the memory cell is lower than the second read level R4_2, sensing data stored in the latch LATS may be maintained and the second sub-node QS may maintain a high level. Alternatively, when a level of a threshold voltage of a memory cell is lower than the first read level R4_1 and is higher

than the second read level R4_2, the second sub-node QS may be set to have a low level.

[00107] The main read voltage R4 may be applied to the word line WL corresponding to the selected page during a period t7.

5 The main read voltage R4 may correspond to the main read level shown in FIG. 8.

[00108] The PMOS transistor P2 of the clamp circuit 235A may be turned on or off in response to a potential of the second sub-node QS. For example, when a level of a threshold voltage of a
10 memory cell is higher than the first read level R4_1 or lower than the second read level R4_2 during a previous sensing operation, because a potential of the second sub-node QS is a high level, the PMOS transistor P2 may be turned off. Accordingly, a precharge operation of the bit line BL1 is not
15 performed, therefore, a potential of the bit line BL1 may become a ground level GND.

[00109] Alternatively, when a level of a threshold voltage of a memory cell is lower than the first read level R4_1 and higher than the second read level R4_2 during a previous sensing
20 operation, because a potential of the second sub-node QS has a low level, the PMOS transistor P2 may be turned on. Accordingly, the bit line BL1 may be precharged to a predetermined level.

[00110] When a precharge operation of the bit line BL1 was not performed during the previous period, that is, the period t7,

and the potential of the bit line BL1 became the ground level GND, even when a sensing operation on the main read level is performed during a period t8, sensed data may be maintained in the latch LATM without change. In other words, when a level of
5 a threshold voltage of a memory cell coupled to the bit line BL1 is higher than the first read level R4_1, the first main node QM_N may maintain a low level, and when the level of the threshold voltage of the memory cell coupled to the bit line BL1 is lower than the second read level R4_2, the first main node
10 QM_N may maintain a high level.

[00111] Alternatively, when the precharge operation of the bit line BL1 was performed during the period t7, the PMOS transistor P3 may be turned off in response to the internal sensing node precharge signal SA_PRECH_N during the period t8.
15 Accordingly, a cell current of the bit line BL1 may vary according to a threshold voltage of a memory cell coupled to the bit line BL1. The NMOS transistor N4 may maintain a turn-on state during the sensing time Sensing time of the period t8 and may then be turned off in response to the node coupling signal
20 TRANSO. Accordingly, a potential of the sensing node SO may be maintained at a high level or may be discharged to a low level according to a cell current of the bit line BL1. Subsequently, the main setup signal MSET having a high level may be applied to the main latch reset/setup circuit RSEM, such

that the first main node QM_N of the latch LATM maintains a high level or is set up to have a low level. In other words, when a level of a threshold voltage of a memory cell coupled to the bit line BL1 is higher than the main read level R4, the first main node QM_N may be set up to have a low level, and when the level of the threshold voltage of the memory cell coupled to the bit line BL1 is lower than the main read level R4, the first main node QM_N may maintain a high level.

[00112] As described above, according to an embodiment, a sensing operation performed by applying the main read voltage R4 may be performed after a masking process is performed on bit lines of memory cells corresponding to the region A and the region B according to sensing results of a sensing operation performed by applying the first read level voltage R4_1 greater than the main read voltage R4 to a word line and a sensing operation performed by applying the second read level voltage R4_2 smaller than the main read voltage R4 to the word line.

[00113] FIG. 12 is a waveform of signals illustrating an operation of a page buffer according to another embodiment.

[00114] An operation of a page buffer according to another embodiment is described below with reference to FIGs. 5, 8 to 10, and 12. When a read operation is performed, a plurality of page buffers operate in a similar manner. Accordingly, the page buffer PB1 is described as an example.

[00115] In another embodiment, a read operation using the fourth read voltage R4 among the read operations using a plurality of read voltages is described as an example.

[00116] The page buffer PB1 may perform an initialization operation during the period t1. For example, the PMOS transistor P5 may be turned on in response to the precharge signal PRECHSO_N to apply the power voltage VEXT to the sensing node SO. Accordingly, the NMOS transistor N17 of the second discharge circuit 241 may be turned on to apply the ground power Vss to the common node COM. Subsequently, the main reset signal MRST having a high level may be applied to the main latch reset/setup circuit RSEM to initialize the second main node QM of the latch LATM to a low level. In addition, the sub-reset signal SRST having a high level may be applied to the sub-latch reset/setup circuit RSES to initialize the second sub-node QS of the latch LATS to a low level.

[00117] The main read voltage R4 corresponding to a main read level may be applied to the word line WL corresponding to the selected page during the period t2.

[00118] The PMOS transistor P2 of the clamp circuit 235A may be turned on in response to a potential of the second sub-node QS, and the PMOS transistor P3 of the clamp circuit 235A may be turned on in response to the internal sensing node precharge signal SA_PRECH_N to apply the core voltage VCORE to the

current sensing node CSO. The NMOS transistor N1 of the bit line coupling circuit 231 may be turned on in response to the bit line select signal PB_SELBL and the NMOS transistor N3 of the page buffer sensing circuit 233 may be turned on in response to the page buffer sensing signal PB_SENSE to electrically couple the bit line BL1 to the current sensing node CSO to which the core voltage V_{CORE} is applied. The page buffer sensing signal PB_SENSE may be a first voltage V1. Accordingly, the bit line BL1 may be precharged to a potential of a first bit line voltage VBL_R4_1. The first bit line voltage VBL_R4_1 may correspond to the first read level R4_1 shown in FIG. 8.

[00119] The PMOS transistor P3 may be turned off in response to the internal sensing node precharge signal SA_PRECH_N during the period t3. Accordingly, a cell current of the bit line BL1 may vary according to a threshold voltage of a memory cell coupled to the bit line BL1. The cell current of the bit line BL1 may be affected by a precharge level of the bit line BL1. For example, when a precharge level of a bit line is high in a state where the same read voltage is applied to a word line, a cell current may be increased and have an effect of increasing a read level. In other words, when a sensing operation is performed by adjusting the precharge level of the bit line BL1 to a potential of the first bit line voltage VBL_R4_1 in a state where the fourth read voltage R4 is applied to the word line, a sensing result with

respect to the first read level R4_1 may be obtained. The NMOS transistor N4 may maintain a turn-on state during the sensing time Sensing time of the period t3 and may then be turned off in response to the node coupling signal TRANSO. Accordingly, a
5 potential level of the sensing node SO may be maintained at a high level or may be discharged to a low level according to a cell current of the bit line BL1. Subsequently, the main setup signal MSET having a high level may be applied to the main latch reset/setup circuit RSEM, such that the first main node QM_N of
10 the latch LATM maintains a high level or is set up to have a low level. In other words, when a threshold voltage of a memory cell coupled to the bit line BL1 is greater than the first read level R4_1, the first main node QM_N may be set up to have a low level, and when the threshold voltage of the memory cell
15 coupled to the bit line BL1 is smaller than the first read level R4_1, the first main node QM_N may maintain a high level.

[00120] The PMOS transistor P2 of the clamp circuit 235A may be turned on in response to a potential of the second sub-node QS, and the PMOS transistor P3 of the clamp circuit 235A may
20 be turned on in response to the internal sensing node precharge signal SA_PRECH_N to apply the core voltage VCORE to the current sensing node CSO during the period t4. The NMOS transistor N1 of the bit line coupling circuit 231 may be turned on in response to the bit line select signal PB_SELBL and the

NMOS transistor N3 of the page buffer sensing circuit 233 may be turned on in response to the page buffer sensing signal PB_SENSE to electrically couple the bit line BL1 to the current sensing node CSO to which the core voltage V_{CORE} is applied.

5 The page buffer sensing signal PB_SENSE may be a second voltage V₂. The second voltage V₂ may be lower than the first voltage V₁. Accordingly, the bit line BL1 may be precharged to a potential of a second bit line voltage VBL_R4_2. The second bit line voltage VBL_R4_2 may correspond to the second read
10 level R4_2 shown in FIG. 9.

[00121] The PMOS transistor P3 may be turned off in response to the internal sensing node precharge signal SA_PRECH_N during the period t₅. Accordingly, a cell current of the bit line BL1 may vary according to a threshold voltage of a memory cell
15 coupled to the bit line BL1. The cell current of the bit line BL1 may be affected by a precharge level of the bit line BL1. In other words, when a sensing operation is performed by adjusting the precharge level of the bit line BL1 to a potential of the second bit line voltage VBL_R4_2 in a state where the fourth
20 read voltage R4 is applied to the word line, a sensing result with respect to the second read level R4_2 may be obtained. The NMOS transistor N4 may maintain a turn-on state during the sensing time Sensing time of the period t₅ and may then be turned off in response to the node coupling signal TRANSO.

Accordingly, a potential level of the sensing node SO may be maintained at a high level or may be discharged to a low level according to a cell current of the bit line BL1. The reset signal PBRST having a high level may be applied to the sub-latch reset/setup circuit RSES to set the first sub-node QS_N of the latch LATS to a low level. Subsequently, the sub-reset signal SRST having a high level may be applied to the sub-latch reset/setup circuit RSES, such that the second sub-node QS of the latch LATS maintains a high level or is set up to have a low level. In other words, when a threshold voltage of a memory cell coupled to the bit line BL1 is greater than the second read level R4_2, the second sub-node QS may be set up to have a low level, and when the threshold voltage of the memory cell coupled to the bit line BL1 is smaller than the second read level R4_2, the second sub-node QS may maintain a high level.

[00122] Sensing data stored in the latch LATM may be transmitted to the latch LATS during the period t6. Accordingly, data based on the sensing data that is sensed during the period t5 and the sensing data that is sensed during the period t3 may be newly stored in the latch LATS. For example, the PMOS transistor P5 may be turned on in response to the precharge signal PRECHSO_N to apply the power voltage VEXT to the sensing node SO. Accordingly, the sensing node SO may be precharged to a predetermined level. Subsequently, when the

NMOS transistor N9 is turned on in response to the main data transmission signal TRANM, a potential level of the sensing node SO may be maintained at a precharge level or may be discharged to a low level according to a potential level of the first main node QM_N. Subsequently, the sub-setup signal SSET having a high level may be applied to the sub-latch reset/setup circuit RSES, such that the second sub-node QS of the latch LATS maintains a previous level or is set up to have a high level.

[00123] For example, when a threshold voltage of a memory cell is greater than the first read level R4_1, sensing data stored in the latch LATM may be transmitted to the latch LATS and the second sub-node QS of the latch LATS may become a high level. In addition, when the threshold voltage of the memory cell is smaller than the second read level R4_2, sensing data stored in the latch LATS may be maintained and the second sub-node QS may maintain a high level. Alternatively, when a threshold voltage of a memory cell is smaller than the first read level R4_1 and is greater than the second read level R4_2, the second sub-node QS may become a low level.

[00124] The PMOS transistor P2 of the clamp circuit 235A may be turned on or off in response to a potential of the second sub-node QS during the period t7. For example, when a level of a threshold voltage of a memory cell is higher than the first read level R4_1 or lower than the second read level R4_2 during a

previous sensing operation, because a potential of the second sub-node QS has a high level, the PMOS transistor P2 may be turned off. Accordingly, a precharge operation of the bit line BL1 is not performed, therefore, a potential of the bit line BL1 may become the ground level GND.

[00125] Alternatively, when a level of a threshold voltage of a memory cell is lower than the first read level R4_1 and higher than the second read level R4_2 during a previous sensing operation, because a potential of the second sub-node QS has a low level, the PMOS transistor P2 may be turned on. The NMOS transistor N1 of the bit line coupling circuit 231 may be turned on in response to the bit line select signal PB_SELBL and the NMOS transistor N3 of the page buffer sensing circuit 233 may be turned on in response to the page buffer sensing signal PB_SENSE to electrically couple the bit line BL1 to the current sensing node CSO to which the core voltage V_{CORE} is applied. The page buffer sensing signal PB_SENSE may be a third voltage V₃. Accordingly, the bit line BL1 may be precharged to a potential of the main bit line voltage V_{BL_R4}. The main bit line voltage V_{BL_R4} may correspond to the main read level R4 shown in FIG. 8. The third voltage V₃ may be smaller than the first voltage V₁ and greater than the second voltage V₂.

[00126] When a precharge operation of the bit line BL1 was not performed during the previous period, that is, the period t₇,

and the potential level of the bit line BL1 became the ground level GND, even when a sensing operation on a main read level is performed during the period t8, sensed data may be maintained in the latch LATM without change. In other words, when a threshold voltage of a memory cell coupled to the bit line BL1 is greater than the first read level R4_1, the first main node QM_N may maintain a low level, and when the threshold voltage of the memory cell is smaller than the second read level R4_2, the first main node QM_N may maintain a high level.

[00127] Alternatively, when a precharge operation of the bit line BL1 was performed during the period t7, the PMOS transistor P3 may be turned off in response to the internal sensing node precharge signal SA_PRECH_N during the period t8. Accordingly, a cell current of the bit line BL1 may vary according to a threshold voltage of a memory cell coupled to the bit line BL1. The NMOS transistor N4 may maintain a turn-on state during the sensing time Sensing time of the period t8 and may then be turned off in response to the node coupling signal TRANSO. Accordingly, a potential level of the sensing node SO may be maintained at a high level or may be discharged to a low level according to a cell current of the bit line BL1. Subsequently, the main setup signal MSET having a high level may be applied to the main latch reset/setup circuit RSEM, such that the first main node QM_N of the latch LATM maintains a

high level or is set up to have a low level. In other words, when a level of a threshold voltage of a memory cell coupled to the bit line BL1 is higher than the main read level R4, the first main node QM_N may become a low level, and when the level of the threshold voltage of the memory cell coupled to the bit line BL1 is lower than the main read level R4, the first main node QM_N may maintain a high level.

[00128] As described above, according to another embodiment, a sensing operation corresponding to the main read level R4 may be performed after a masking process is performed on bit lines of memory cells corresponding to the region A and the region B according to sensing results of a sensing operation corresponding to the first read level R4_1 and a sensing operation corresponding to the second read level R4_2 by changing a precharge level of the bit line BL1 in a state where the main read voltage R4 corresponding to the main read level is applied to a word line.

[00129] FIG. 13 is a waveform diagram of signals illustrating an operation of a page buffer according to another embodiment.

[00130] An operation of a page buffer according to another embodiment is described below with reference to FIGs. 5, 8 to 10, and 13. When a read operation is performed, a plurality of page buffers operate in a similar manner. Accordingly, the page buffer PB1 is described as an example.

[00131] In another embodiment, a read operation using the fourth read voltage R4 among the read operations using a plurality of read voltages is described as an example.

[00132] The page buffer PB1 may perform an initialization operation during the period t1. For example, the PMOS transistor P5 may be turned on in response to the precharge signal PRECHSO_N to apply the power voltage VEXT to the sensing node SO. Accordingly, the NMOS transistor N17 of the second discharge circuit 241 may be turned on to apply the ground power Vss to the common node COM. Subsequently, the main reset signal MRST having a high level may be applied to the main latch reset/setup circuit RSEM to initialize the second main node QM of the latch LATM to a low level. In addition, the sub-reset signal SRST having a high level may be applied to the sub-latch reset/setup circuit RSES to initialize the second sub-node QS of the latch LATS to a low level.

[00133] The main read voltage R4 corresponding to the main read level may be applied to the word line WL corresponding to the selected page during the period t2.

[00134] The PMOS transistor P2 of the clamp circuit 235A may be turned on in response to a potential of the second sub-node QS and the PMOS transistor P3 of the clamp circuit 235A may be turned on in response to the internal sensing node precharge signal SA_PRECH_N to apply the core voltage VCORE to the

current sensing node CSO. The NMOS transistor N1 of the bit line coupling circuit 231 may be turned on in response to the bit line select signal PB_SELBL and the NMOS transistor N3 of the page buffer sensing circuit 233 may be turned on in response to the page buffer sensing signal PB_SENSE to electrically couple the bit line BL1 to the current sensing node CSO to which the core voltage V_{CORE} is applied.

[00135] The PMOS transistor P3 may be turned off in response to the internal sensing node precharge signal SA_PRECH_N during the period t₃. Accordingly, a cell current of the bit line BL1 may vary according to a threshold voltage of a memory cell coupled to the bit line BL1. A sensing operation on the first read level R_{4_1} may be performed during a first sensing time Sensing time₁ by controlling a turn-on period of the node coupling signal TRANSO. When the first sensing time Sensing time₁ is adjusted to be relatively long, a reference current I_{trip} of a page buffer may be changed, and thus a sensing operation on the first read level R_{4_1} may be performed. For example, when a sensing time is increased in a state where the same read voltage is applied to a word line and a bit line is precharged to the same potential level, an effect of increasing a read level may be obtained. In other words, when a sensing operation is performed for the first sensing time Sensing time₁ in a state where the fourth read voltage R₄ is applied to a word line and

the bit line BL1 is precharged to a predetermined level, a sensing result with respect to the first read level R4_1 may be obtained. The NMOS transistor N4 may maintain a turn-on state during the first sensing time Sensing time1 of the period t3 and
5 may then be turned off in response to the node coupling signal TRANSO. Accordingly, a potential level of the sensing node SO may be maintained at a high level or may be discharged to a low level according to a cell current of the bit line BL1. Subsequently, the main setup signal MSET having a high level
10 may be applied to the main latch reset/setup circuit RSEM, such that the first main node QM_N of the latch LATM maintains a high level or is set up to have a low level. In other words, when a threshold voltage of a memory cell coupled to the bit line BL1 is greater than the first read level R4_1, the first main node
15 QM_N may be set up to have a low level , and when the threshold voltage of the memory cell coupled to the bit line BL1 is smaller than the first read level R4_1, the first main node QM_N may maintain a high level.

[00136] The PMOS transistor P2 of the clamp circuit 235A may
20 be turned on in response to a potential of the second sub-node QS, and the PMOS transistor P3 of the clamp circuit 235A may be turned on in response to the internal sensing node precharge signal SA_PRECH_N to apply the core voltage VCORE to the current sensing node CSO during the period t4. The NMOS

transistor N4 may be turned on in response to the node coupling signal TRANSO to precharge the sensing node SO. Only the sensing node SO may be precharged without performing a precharge operation on the bit line BL1 during the period t4.

5 **[00137]** The PMOS transistor P3 may be turned off in response to the internal sensing node precharge signal SA_PRECH_N during the period t5. Accordingly, a cell current of the bit line BL1 may vary according to a threshold voltage of a memory cell coupled to the bit line BL1. A sensing operation on the second
10 read level R4_2 may be performed during a second sensing time Sensing time2 by controlling a turn-on period of the node coupling signal TRANSO. When the second sensing time Sensing time2 is adjusted to be relatively short, the reference current Itrip of a page buffer may be changed, and thus a sensing
15 operation on the second read level R4_2 may be performed. The second sensing time Sensing time2 may be shorter than the first sensing time Sensing time1. The NMOS transistor N4 may maintain a turn-on state during the second sensing time Sensing time2 of the period t5 and may then be turned off in response to
20 the node coupling signal TRANSO. Accordingly, a potential level of the sensing node SO may be maintained at a high level or may be discharged to a low level according to a cell current of the bit line BL1. The reset signal PBRST having a high level may be applied to the sub-latch reset/setup circuit RSES to set the

first sub-node QS_N of the latch LATS to a low level. Subsequently, the sub-reset signal SRST having a high level may be applied to the sub-latch reset/setup circuit RSES, such that the second sub-node QS of the latch LATS maintains a high level
5 or is set up to have a low level. In other words, when a threshold voltage of a memory cell coupled to the bit line BL1 is greater than the second read level R4_2, the second sub-node QS may be set up to have a low level, and when the threshold voltage of the memory cell coupled to the bit line BL1 is smaller
10 than the second read level R4_2, the second sub-node QS may maintain a high level.

[00138] Sensing data stored in the latch LATM may be transmitted to the latch LATS during the period t6. Accordingly, data based on the sensing data that is sensed during the period
15 t5 and the sensing data that is sensed during the period t3 may be newly stored in the latch LATS. For example, the PMOS transistor P5 may be turned on in response to the precharge signal PRECHSO_N to apply the power voltage VEXT to the sensing node SO. Accordingly, the sensing node SO may be
20 precharged to a predetermined level. Subsequently, when the NMOS transistor N9 is turned on in response to the main data transmission signal TRANM, a potential level of the sensing node SO may be maintained at a precharge level or may be discharged to a low level according to a potential level of the

first main node QM_N. Subsequently, the sub-setup signal SSET having a high level may be applied to the sub-latch reset/setup circuit RSES, such that the second sub-node QS of the latch LATS maintains a previous level or is set up to have a high level.

5 **[00139]** For example, when a level of a threshold voltage of a memory cell is higher than the first read level R4_1, sensing data stored in the latch LATM may be transmitted to the latch LATS and the second sub-node QS of the latch LATS may become a high level. In addition, when a level of a threshold voltage of
10 a memory cell is lower than the second read level R4_2, sensing data stored in the latch LATS may be maintained and the second sub-node QS may maintain a high level. Alternatively, when a level of a threshold voltage of a memory cell is lower than the first read level R4_1 and is higher than the second read level
15 R4_2, the second sub-node QS may become a low level.

20 **[00140]** The PMOS transistor P2 of the clamp circuit 235A may be turned on or off in response to a potential of the second sub-node QS during the period t7. For example, when a level of a threshold voltage of a memory cell is higher than the first read level R4_1 or lower than the second read level R4_2 during a previous sensing operation, because a potential of the second sub-node QS has a high level, the PMOS transistor P2 may be turned off. Accordingly, a precharge operation of the bit line BL1 is not performed, therefore, a potential of the bit line BL1

may become the ground level GND.

[00141] Alternatively, when a level of a threshold voltage of a memory cell is lower than the first read level R4_1 and higher than the second read level R4_2 during a previous sensing operation, because a potential of the second sub-node QS has a low level, the PMOS transistor P2 may be turned on. The NMOS transistor N1 of the bit line coupling circuit 231 may be turned on in response to the bit line select signal PB_SELBL and the NMOS transistor N3 of the page buffer sensing circuit 233 may be turned on in response to the page buffer sensing signal PB_SENSE to electrically couple the bit line BL1 to the current sensing node CSO to which the core voltage V_{CORE} is applied. Accordingly, the bit line BL1 may be precharged to a predetermined level.

[00142] When a precharge operation of the bit line BL1 was not performed during the previous period, that is, the period t₇, and the potential level of the bit line BL1 became the ground level GND, even when a sensing operation on a main read level is performed during the period t₈, sensed data may be maintained in the latch LATM without change. In other words, when a threshold voltage of a memory cell coupled to the bit line BL1 is greater than the first read level R4_1, the first main node QM_N may maintain a low level, and when the threshold voltage of the memory cell coupled to the bit line BL1 is smaller than the

second read level R4_2, the first main node QM_N may maintain a high level.

[00143] Alternatively, when a precharge operation of the bit line BL1 was performed during the period t7, the PMOS transistor P3 may be turned off in response to the internal sensing node precharge signal SA_PRECH_N during the period t8. Accordingly, a cell current of the bit line BL1 may vary according to a threshold voltage of a memory cell coupled to the bit line BL1. The NMOS transistor N4 may maintain a turn-on state during a third sensing time Sensing time3 of the period t8 and may then be turned off in response to the node coupling signal TRANSO. Accordingly, a potential level of the sensing node SO may be maintained at a high level or may be discharged to a low level according to a cell current of the bit line BL1. A sensing operation on the main read level R4 may be performed during the third sensing time Sensing time3 by adjusting a turn-on period of the node coupling signal TRANSO. The third sensing time Sensing time3 may be shorter than the first sensing time Sensing time1 and longer than the second sensing time Sensing time2. When the third sensing time Sensing time3 is adjusted to be shorter than the first sensing time Sensing time1 and longer than the second sensing time Sensing time2, the reference current Itrip of a page buffer may be changed, and thus a sensing operation on the main read level R4 may be performed.

[00144] Subsequently, the main setup signal MSET having a high level may be applied to the main latch reset/setup circuit RSEM, such that the first main node QM_N of the latch LATM maintains a high level or is set up to have a low level. In other words, when a level of a threshold voltage of a memory cell coupled to the bit line BL1 is higher than the main read level R4, the first main node QM_N may become a low level, and when the level of the threshold voltage of the memory cell coupled to the bit line BL1 is lower than the main read level R4, the first main node QM_N may maintain a high level.

[00145] As described above, according to another embodiment, a sensing operation corresponding to the main read level R4 may be performed after a masking process is performed on bit lines of memory cells corresponding to the region A and the region B according to sensing results of a sensing operation corresponding to the first read level R4_1 and a sensing operation corresponding to the second read level R4_2 by adjusting a length of a sensing time in a state where the main read voltage R4 corresponding to the main read level is applied to a word line.

[00146] FIG. 14 is a diagram illustrating another embodiment of a memory system.

[00147] Referring to FIG. 14, a memory system 30000 may be embodied into a cellular phone, a smartphone, a tablet PC, a

personal digital assistant (PDA) or a wireless communication device. The memory system 30000 may include a memory device 1100 and a memory controller 1200 controlling the operations of the memory device 1100. The memory controller
5 1200 may control a data access operation of the memory device 1100, for example, a program operation, an erase operation, or a read operation in response to control of a processor 3100.

[00148] The memory controller 1200 may control data programmed into the memory device 1100 to be output through
10 a display 3200 in response to control of the memory controller 1200.

[00149] A radio transceiver 3300 may exchange a radio signal through an antenna ANT. For example, the radio transceiver 3300 may change the radio signal received through the antenna
15 ANT into a signal which can be processed by the processor 3100. Therefore, the processor 3100 may process the signal output from the radio transceiver 3300 and transfer the processed signal to the memory controller 1200 or the display 3200. The memory controller 1200 may program the signal processed by
20 the processor 3100 into the memory device 1100. In addition, the radio transceiver 3300 may change a signal output from the processor 3100 to a radio signal and output the radio signal to an external device through the antenna ANT. A control signal for controlling the operations of the processor 3100 or data to

be processed by the processor 3100 may be input by an input device 3400, and the input device 3400 may include a pointing device, such as a touch pad and a computer mouse, a keypad, or a keyboard. The processor 3100 may control operations of the display 3200 so that the data output from the controller 1200, the data output from the radio transceiver 3300, or the data output from the input device 3400 may be displayed on the display 3200.

[00150] According to an embodiment, the memory controller 1200 controlling the operations of the memory device 1100 may form part of the processor 3100, or be formed as a separate chip from the processor 3100. Further, the memory device 1100 may be formed through the examples of the memory controller 1100 shown in FIG. 2.

[00151] FIG. 15 is a diagram illustrating another embodiment of a memory system.

[00152] Referring to FIG. 15, a memory system 40000 may be embodied into a personal computer (PC), a tablet PC, a net-book, an e-reader, a personal digital assistant (PDA), a portable multimedia player (PMP), an MP3 player, or an MP4 player.

[00153] The memory system 40000 may include the memory device 1100 and the memory controller 1200 controlling a data processing operation of the memory device 1100.

[00154] A processor 4100 may output data stored in the

memory device 1100 through a display 4300 according to data input through an input device 4200. Examples of the input device 4200 may include a pointing device, such as a touch pad or a computer mouse, a keypad, or a keyboard.

5 **[00155]** The processor 4100 may control the general operations of the memory system 40000 and control the operations of the memory controller 1200. According to an embodiment, the memory controller 1200 controlling the operations of the memory device 1100 may form part of the
10 processor 4100, or be formed as a separate chip from the processor 4100. Further, the memory device 1100 may be formed through the examples of the memory controller 1100 shown in FIG. 2.

15 **[00156]** FIG. 16 is a diagram illustrating another embodiment of a memory system.

20 **[00157]** Referring to FIG. 16, a memory system 50000 may be embodied into an image processing device, for example, a digital camera, a cellular phone with a digital camera attached thereto, a smartphone with a digital camera attached thereto, or a tablet PC with a digital camera attached thereto.

25 **[00158]** The memory system 50000 may include the memory device 1100 and the memory controller 1200 controlling a data processing operation of the memory device 1100, for example, a program operation, an erase operation, or a read operation.

[00159] An image sensor 5200 of the memory system 50000 may convert an optical image into digital signals, and the digital signals may be transferred to a processor 5100 or the memory controller 1200. In response to control of the processor 5100,
5 the digital signals may be output through a display 5300 or stored in the memory device 1100 through the controller 1200. In addition, the data stored in the memory device 1100 may be output through the display 5300 according to control of the processor 5100 or the memory controller 1200.

10 **[00160]** According to an embodiment, the memory controller 1200 controlling the operations of the memory device 1100 may form part of the processor 5100, or be formed as a separate chip from the processor 5100. Further, the memory device 1100 may be formed through the examples of the memory controller 1100
15 shown in FIG. 2.

[00161] FIG. 17 is a diagram illustrating another embodiment of a memory system.

[00162] Referring to FIG. 17, a memory system 70000 may be embodied into a memory card or a smart card. The memory
20 system 70000 may include the memory device 1100, the memory controller 1200, and a card interface 7100.

[00163] The memory controller 1200 may control data exchange between the memory device 1100 and the card interface 7100. According to an embodiment, the card interface

7100 may be, but is not limited to, a secure digital (SD) card interface or a multi-media card (MMC) interface. Further, the memory controller 1200 may be formed through the example of the memory controller 1200 shown in FIG. 2.

5 **[00164]** The card interface 7100 may interface data exchange between a host 60000 and the memory controller 1200 according to a protocol of the host 60000. According to an embodiment, the card interface 7100 may support a Universal Serial Bus (USB) protocol and an InterChip (IC)-USB protocol. The card
10 interface may refer to hardware capable of supporting a protocol which is used by the host 60000, software installed in the hardware, or a signal transmission method.

[00165] When the memory system 70000 is connected to an host interface 6200 of the host 60000, such as a PC, a tablet PC,
15 a digital camera, a digital audio player, a cellular phone, console video game hardware, or a digital set-top box, the host interface 6200 may perform data communication with the memory device 1100 through the card interface 7100 and the memory controller 1200 in response to control of a microprocessor 6100. Further,
20 the memory device 1100 may be formed through the examples of the memory controller 1100 shown in FIG. 2.

[00166] According to the present disclosure, the reliability of a read operation of a memory device may be improved by suppressing noise caused by an adjacent bit line during the read

operation.

WHAT IS CLAIMED IS:

1. A memory device, comprising:

5 a memory cell array including memory cells that are programmed into a plurality of program states;

a peripheral circuit configured to perform a read operation on the memory cell array; and

control logic configured to control the peripheral circuit to perform:

10 the read operation; and

a masking process on first memory cells having a threshold voltage level higher than a first read level and second memory cells having a threshold voltage level lower than a second read level among the memory cells during the read operation, the
15 second read level being lower than the first read level.

2. The memory device of claim 1, wherein the first read level is higher than a main read level and the second read level is lower than the main read level.

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3. The memory device of claim 2, wherein the peripheral circuit comprises:

a voltage generating circuit configured to apply a read voltage to a selected word line among word lines of the memory

cell array; and

a page buffer group configured to precharge bit lines of the memory cell array and then sense change in current of the bit lines of the memory cell array.

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4. The memory device of claim 3, wherein the page buffer group applies a ground voltage to first bit lines to which the first memory cells or the second memory cells are coupled, among the bit lines coupled to the memory cell array, and
10 performs the masking process on the first bit lines.

5. The memory device of claim 3, wherein the control logic controls the peripheral circuit to perform a first sensing operation in which the first memory cells are sensed, a second
15 sensing operation in which the second memory cells are sensed, and a third sensing operation in which the masking process is performed on the first and second memory cells and then the memory cells except for the first and second memory cells are sensed.

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6. The memory device of claim 5, wherein the voltage generating circuit applies a first read level voltage corresponding to the first read level to the selected word line during the first sensing operation, applies a second read level voltage

corresponding to the second read level to the selected word line during the second sensing operation, and applies a main read voltage corresponding to the main read level to the selected word line during the third sensing operation.

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7. The memory device of claim 6, wherein the first read level voltage is greater than the main read voltage and the second read level voltage is less than the main read voltage.

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8. The memory device of claim 6, wherein the page buffer group applies a ground voltage to first bit lines corresponding to the first or second memory cells during the third sensing operation based on sensing data obtained from results of the first sensing operation and the second sensing operation, and precharges second bit lines, that is, the bit lines except for the first bit lines, to a predetermined level.

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9. The memory device of claim 5, wherein the voltage generating circuit applies a main read voltage to the selected word line during the first, second, and third sensing operations, and

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wherein the page buffer group precharges the bit lines to a first bit line voltage corresponding to the first read level during the first sensing operation, precharges the bit lines to a second

bit line voltage corresponding to the second read level during the second sensing operation, and precharges second bit lines, that is, the bit lines except for first bit lines corresponding to the first and second memory cells, to a third bit line voltage
5 corresponding to the main read level during the third sensing operation.

10. The memory device of claim 9, wherein the first bit line voltage is greater than the third bit line voltage and the
10 second bit line voltage is less than the third bit line voltage.

11. The memory device of claim 5, wherein the voltage generating circuit applies a main read voltage to the selected word line during the first, second, and third sensing operations,
15 and

wherein the page buffer group senses the bit lines using a first reference current for a first sensing time during the first sensing operation, senses the bit lines using a second reference current for a second sensing time during the second sensing
20 operation, and senses second bit lines, that is, the bit lines except for first bit lines corresponding to the first or second memory cells, using a third reference current for a third sensing time during the third sensing operation.

12. The memory device of claim 11, wherein the first sensing time is longer than the third sensing time and the second sensing time is shorter than the third sensing time.

5 13. A memory device comprising:

 a page including a plurality of memory cells coupled in common to one word line;

 a peripheral circuit configured to perform a read operation on the page; and

10 control logic configured to control the peripheral circuit to perform the read operation,

 wherein, during the read operation, the control logic controls the peripheral circuit to perform:

 a first sensing operation in which first memory cells having
15 a threshold voltage level higher than or equal to a first read level that is higher than a main read level, among the plurality of memory cells, are sensed;

 a second sensing operation in which second memory cells having a threshold voltage level lower than or equal to a second
20 read level that is lower than the main read level, among the plurality of memory cells, are sensed; and

 a third sensing operation in which the plurality of memory cells are sensed in a state where a masking process is performed on the first memory cells and the second memory cells.

14. The memory device of claim 13, wherein the peripheral circuit changes a read voltage to be applied to the word line during the first, second, and third sensing operations.

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15. The memory device of claim 13, wherein the peripheral circuit changes a precharge level for precharging bit lines coupled to the memory cells during the first, second, and third sensing operations.

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16. The memory device of claim 13, wherein the peripheral circuit changes a sensing time during the first, second, and third sensing operations.

15 17. A method of operating a memory device, the method comprising:

performing a first sensing operation in which first memory cells having a threshold voltage level higher than or equal to a first read level that is higher than a main read level, among a plurality of memory cells, are sensed;

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performing a second sensing operation in which second memory cells having a threshold voltage level lower than or equal to a second read level that is lower than the main read level, among the plurality of memory cells, are sensed;

performing a masking process on the first memory cells and the second memory cells; and

performing a third sensing operation in which whether a threshold voltage level of the plurality of memory cells is higher
5 or lower than the main read level is sensed.

18. The method of claim 17, wherein a ground voltage is applied to bit lines coupled to the first memory cells or the second memory cells during the third sensing operation by
10 performing the masking process.

19. The method of claim 17, wherein a read voltage applied to word lines during the first, second, and third sensing operations varies among the first, second, and third sensing
15 operations.

20. The method of claim 17, wherein a precharge level for precharging bit lines coupled to the memory cells during the first, second, and third sensing operations varies among the first,
20 second, and third sensing operations.

21. The method of claim 17, wherein a sensing time varies among the first, second, and third sensing operations.