ABSTRACT

According to an embodiment, an information processing device controls access from n (n being an integer equal to or greater than 2) MPUs to a shared memory. The information processing device includes a control unit. The control unit analyzes an access pattern to the shared memory based on access requests to the shared memory received in parallel from the n MPUs in a same access phase, and sequentially processes, in the access phase, the received m (m being a natural number equal to or less than n) access requests in order based on the analyzed access pattern.