Claims

1. A device, comprising:

a semiconductor substrate having a first substrate surface and a second substrate surface;

a dielectric on the semiconductor substrate, the dielectric having a first dielectric surface and a second dielectric surface, wherein the second dielectric surface is in direct contact with the first substrate surface;

a depression in the dielectric;

an aperture through the dielectric and at least a portion of the semiconductor substrate;

a conductive material having a first portion in the depression and a second portion in the aperture;

a conductive interconnect structure positioned within the dielectric and electrically coupled to the conductive material in the aperture, wherein the conductive interconnect structure is laterally positioned between the conductive material and a trace positioned within the dielectric;

a passivation material formed on the second substrate surface, wherein the passivation material is formed with an opening;

a bond site formed through the opening; and

a conductive pillar electrically coupled to the bond site.

2. The device of claim 1 wherein:

the depression extends between the first dielectric surface and the second dielectric surface;

the aperture extends from the first dielectric surface to the second substrate surface; and

the first and second portions of the conductive material are generally homogeneous.

3. The device of claim 1, further comprising:
a solder material positioned between the bond site and the conductive pillar.

4. The device of claim 1, wherein the aperture has a depth of at least 50 microns from the first dielectric surface and an aspect ratio of at least 5:1.

5. The device of claim 1, wherein the depression has a depth of about 0.3 to about 0.5 microns from the first dielectric surface.

6. The device of claim 1, wherein the first and second portions of the conductive material include copper.

7. The device of claim 1, wherein the first and second portions of the conductive material are generally contiguous.

8. The device of claim 1, wherein the first and second portions of the conductive material do not include a physical boundary between each other.

9. The device of claim 1, wherein the first and second portions of the conductive material are formed in one single processing stage such that a sacrificial portion of the conductive material extends between the first and second portions.

10. The device of claim 1, wherein the aperture has a first lateral dimension, and wherein the opening has a second lateral dimension smaller than the first lateral dimension, and wherein the conductive pillar has a third lateral dimension greater than the first lateral dimension.

11. A semiconductor device, comprising:

a substrate having a first substrate surface and a second substrate surface;

a dielectric on the substrate, the dielectric having a first dielectric surface and a second dielectric surface, wherein the second dielectric surface is in contact with the first substrate surface;

a depression formed in the dielectric;

an aperture through the dielectric and at least a portion of the substrate;

a conductive material having a first portion in the depression and a second portion in the aperture;

a conductive interconnect structure in the dielectric and electrically coupled to the conductive material, wherein the conductive interconnect structure is laterally positioned between the conductive material and a trace positioned within the dielectric;

a passivation material formed on the second substrate surface, wherein the passivation material is formed with an opening;

a bond site formed through the opening; and

a conductive pillar electrically coupled to the bond site.

12. The semiconductor device of claim 11, wherein the aperture has an open end at the first dielectric surface and a closed end in the substrate toward the second substrate surface, and wherein a first cross-sectional area of the aperture is generally the same as a second cross-sectional area of the aperture at the closed end.

13. The semiconductor device of claim 11, further comprising:

an insulation material positioned in the aperture and on the first dielectric surface of the dielectric.

14. The semiconductor device of claim 11, further comprising: a solder material positioned between the bond site and the conductive pillar.

15. The semiconductor device of claim 11, wherein the aperture has a first lateral dimension, and wherein the opening has a second lateral dimension smaller than the first lateral dimension, and wherein the conductive pillar has a third lateral dimension greater than the first lateral dimension.

16. A semiconductor wafer, comprising:

a substrate having a first substrate surface and a second substrate surface;

a dielectric on the substrate, the dielectric having a first dielectric surface and a second dielectric surface, wherein the second dielectric surface is in contact with the first substrate surface;

a plurality of depressions formed in the dielectric;

at least one aperture through the dielectric and at least a portion of the substrate;

a conductive material having a first portion in the plurality of depressions and a second portion in the aperture;

a conductive interconnect structure in the dielectric and electrically coupled to the conductive material, wherein the conductive interconnect structure is laterally positioned between the conductive material and a trace positioned within the dielectric;

a passivation material formed on the second substrate surface, wherein the passivation material is formed with an opening;

a bond site formed through the opening; and

a conductive pillar electrically coupled to the bond site.

17. The semiconductor wafer of claim 16, wherein the aperture has an open end at the first dielectric surface and a closed end in the substrate toward the second substrate surface, and wherein a first cross-sectional area of the aperture is generally the same as a second cross-sectional area of the aperture at the closed end.

18. The semiconductor wafer of claim 16, further comprising: a solder material positioned between the bond site and the conductive pillar.

19. The semiconductor wafer of claim 16, wherein the aperture has a depth of at least 50 microns from the first dielectric surface and an aspect ratio of at least 5:1, and wherein the depression has a depth of about 0.3 to about 0.5 microns from the first dielectric surface.

20. The semiconductor wafer of claim 16, wherein the aperture has a first lateral dimension, and wherein the opening has a second lateral dimension smaller than the first lateral dimension, and wherein the conductive pillar has a third lateral dimension greater than the first lateral dimension.