"An asynchronous centralized internal control system for a central computer and a plurality of peripheral computers"

The present invention relates to an asynchronous centralized internal control system in which a central computer has priority over a plurality of peripheral computers having the same access priority and in which said central computer and said peripheral computers have access to a main memory through a single bus in order to achieve a time sharing function with respect to access to the main memory.

A control system of this type is particularly useful in installations which include several fast-working peripheral computers, especially for the transmission of data, where, in order to unload the central stored-program control computer, a plurality of peripheral exchange units is put to use, each comprising a low-capacity programmed computer carrying out all the elementary functions at a local level.

However, these peripheral computers must, from time to time, have access to a main memory, for example for an exchange of information with the central computer.

In this case the main memory is connected to a single bus, and the control system performs a

time-sharing function in order to achieve access to the memory.

Nevertheless, control systems of this type are generally complex, expensive and slow-working. The purpose of the present invention is to overcome these disadvantages.

According to the present invention there is provided an asynchronous internal control system in which a central computer has priority over a plurality of peripheral computers having the same access priority, and in which said central computer and peripheral computers have access to a main memory through a single bus, said internal control system including: a searching circuit connected in bidirectional manner to the peripheral computers, for detecting a request by one of them to be connected to a single bus for access to the main memory and for determining the address of the peripheral computer which has made the request, the searching circuit comprising a cyclic counter, a multiplexer and a flip-flop, said multiplexer being controlled by said cyclic counter, the cycle of which depends on the total number of said peripheral computers which can be connected to said bus; and a decision circuit connected in bi-directional manner with the searching circuit, the peripheral computers and the central computer, said decision circuit under instructions from the central computer having means for firstly authorizing

the requesting peripheral computer to be connected to said bus, when the bus is free, and secondly giving the order to all the other computers to be disconnected from said bus, the central computer also being disconnected from the bus at a time when there is no transmission sequence in progress with the main memory; whereby a time sharing function is performed with respect to access to the main memory, the cycle of access to the main memory thus being synchronous.

The present invention will now be described

in greater detail with reference to the accompanying drawings, wherein:-

Figure 1 is a block diagram of one preferred form of an asynchronous centralized control system in which a central computer and a plurality of peripheral computers having the same access priority, have access to a main memory through a single bus; and

Figure 2 is a block diagram of part of the control system shown in Figure 1.

Referring first to Figure 1, a central computer 1 is connected to a main memory 2 by means of a transmission bus 3. Peripheral computers 41, 42 and 43 are also connected to the bus 3. In the drawing only three peripheral computers have been illustrated for the sake of clarity but it will be evident that the number of these peripheral computers can be greater than three. For example, in telephony, because of the accepted standards, the number of these peripheral computers is less than or equal to sixteen.

The various computers work in an asynchronous mode, but it is, nevertheless, possible to synchronize them by the addition of a common clock.

Normally, only the central computer 1 has permanent access to the main memory 2 by means of the transmission bus 3, the peripheral computers 41, 42 and 43 being disconnected from the bus 3.

However, when one of the peripheral computers needs to have access to a large memory, for example for an

exchange of information with another computer, authorization must be requested from an authorization device 5 for the time-sharing of the bus 3, to enable the peripheral computer to be connected to the bus, while preventing any interference with the information circulating along the bus 3.

For this purpose, the authorization device 5 comprises a searching circuit 6 which is connected in a bi-directional manner to the peripheral computers 41, 42 and 43, firstly to detect a possible request for access sent out by one of them, and secondly to determine the address of the peripheral computer which has sent out this request.

The address is then transmitted to the various peripheral computers 41, 42 and 43 and the information of the request for access to the bus 3 is transmitted to a decision circuit 7 which also receives information concerning whether or not the bus 3 is occupied by means of its bi-directional link with the peripheral computers. The decision circuit 7 when authorized by the central computer 1 connects the bus 3 to a peripheral computer, when the central computer 1 can be disconnected from the bus 3 without interrupting a transmission sequence in progress with the main memory 2.

When the searching circuit 6 has detected the request, for example sent out by the peripheral computer 42, to be connected to the bus 3, the decision circuit 7 checks with the other peripheral computers that the bus 3 is free, and, if the central computer 1 does not need the main memory 2, it authorizes the computer 42 to be connected to the bus 3 and gives the order to all the other peripheral computers to be disconnected from the bus if they have not already been disconnected.

The searching circuit 6 then continues its functions, and, when the end of occupation of the bus 3 by the peripheral computer 42 is detected, the central computer 1 will again have access to the main memory 2 by means of the bus 3.

As can be seen, the cycle of access to the main memory 2 is asynchronous, and only certain operating signals need to be synchronized for reasons of compatibility between the various peripheral computers.

The transmission of a message from one computer to another is effected by means of a cycle of writing in the main memory 2, which is carried out by the outputting computer, followed by a cycle of reading of the main memory 2, which is carried out by the receiving computer. The junctions required to inform the receiving

computer that it must carry out a cycle of reading the main memory 2 have not been represented in the drawing, since they do not form part of the invention.

Referring now to Figure 2, the authorization device 5 is shown in greater detail. The searching circuit 6 comprises essentially a cyclic counter 61, a multiplexer 62 and a flip-flop 63.

The inputs of the multiplexer 62 are connected to the peripheral computers 41, 42 and 43. The multiplexer 62 is controlled by means of the cyclic counter 61, the cycle of which depends on the total number of peripheral computers which can be connected to the bus 3. In one preferred form, the connection time of the multiplexer to each input line is equal to 200 nanoseconds.

When the request to be connected to the bus, which has been sent out by one of the peripheral computers 41, 42 and 43, has been detected, the flip-flop 63 changes its state and blocks the cyclic counter 61 at the address of that peripheral computer which has sent out the request.

The decision circuit 7 then receives the information by means of the flip-flop 63. Authorization to connect the peripheral computer to the bus is then given in the form of a single signal. As soon as the

bus 3 is free, the computer indicated by the cyclic counter 61 of the searching circuit 6 is connected thereto.

As soon as authorization has been given, the flip-flop 63 is reset to its initial state and the cyclic counter 61 is put into operation again.

In a modified form, a priority of access to the bus 3 can be assigned to certain computers by means of a simple modification made to the searching circuit 6. In addition a monitoring circuit can be added in order to limit the access time to the main memory which is allocated to each peripheral computer.

CLAIMS.

1. An asynchronous internal control system in which a central computer has priority over a plurality of peripheral computers having the same access priority, and in which said central computer and peripheral computers have access to a main memory through a single bus, said internal control system including: a searching circuit connected in bi-directional manner to the peripheral computers, for detecting a request by one of them to be connected to a single bus for access to the main memory and for determining the address of the peripheral computer which has made the request, the searching circuit comprising a cyclic counter, a multiplexer and a flip-flop, said multiplexer being controlled by said cyclic counter, the cycle of which depends on the total number of said peripheral computers which can be connected to said bus; and a decision circuit connected in bi-directional manner with the searching circuit the peripheral computers and the central computer, said decision circuit under instructions from the central computer having means for firstly authorizing the requesting peripheral computer to be connected to said bus, when the bus is free, and secondly giving the order to all the other computers to be disconnected from said bus, the central computer also being disconnected from the bus at a time when there is no transmission sequence in progress with the main memory; whereby a time sharing function is performed with respect to access to the main memory,

the cycle of access to the main memory thus being asynchronous.

2. A control system according to claim 1, wherein said multiplexer has its inputs connected to said peripheral computer and its output connected to the input of said flip-flop, and wherein one output of said flip-flop is connected to an input of the cyclic counter so as to stop said cyclic counter at the address of the peripheral computer which has requested to be connected to said bus.

3. A control system according to claim 2, wherein the output from the flip-flop is connected to the input of said decision circuit, and wherein one output of the decision circuit is connected firstly to an input of said flip-flop so as to reset the latter to its initial state and secondly to the control terminal of said cyclic counter, so as to start the latter again as soon as authorization to connect to said bus has been granted by said decision circuit.

4. An asynchronous internal control system in which a central computer has priority over a plurality of peripheral computers having the same access priority, and in which said central computer and peripheral computers have access to a main memory through a single bus, said internal control system being constructed and arranged to operate substantially as herein described with reference to and as illustrated in the accompanying drawing.

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