

MEMORY ARCHITECTURE PERMITTING SELECTION OF STORAGE DENSITY
AFTER FABRICATION OF ACTIVE CIRCUITRY

ABSTRACT

A generic wafer includes memory units separated by scribe lanes. Memory chips of different storage capacities can be produced from different numbers of memory units on the generic wafer by forming one or more interconnect layer specialized according to a desired storage capacity and cutting the wafer using a sawing pattern according to the desired storage capacity. The specialized layer can be formed using different masks sets that form a different conductive pattern for each storage capacity or forming a generic interconnect structure with fuses that are cut to select the storage capacity of the memory chips

FIG. 1 accompanies the abstract.



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