LOW TEMPERATURE SELECTIVE EPITAXIAL GROWTH OF SILICON GERMANIUM LAYERS

Field of the Invention

The present invention relates generally to a method and means for growing strained or relaxed or graded silicon germanium (SiGe) layers on a semiconductor substrate using a low temperature selective epitaxial growth process.

Background

Selective epitaxial growth (SEG) is a known method for selectively growing a homogeneous or heterogeneous semiconductor layer only in a desired location over an exposed semiconductor surface, while avoiding growth over a surface area that has been masked with an oxide or nitride layer.

In particular, SEG has been used to grow SiGe layers on crystalline substrates, such as single crystalline silicon substrates, while growth on amorphous surfaces, areas masked typically with SiO_2 or Si_3N_4, is inhibited. In other words, the SiGe layer is selectively grown only on the portion of the silicon substrate surface that is exposed through windows in the mask layer. Grown SiGe layers can be either strained or relaxed or graded.

Prior art methods of growing SiGe layers rely on the use of chlorosilanes and germanes as the source gases (vapors) for the deposited layer. In particular, SiGe layers may be deposited using dichlorosilane and germane as the precursor materials in accordance with the following chemical reaction equation.

$$SiH_2Cl_2 + GeH_4 \longrightarrow SiGe + 2HCl + 2H_2$$

However, use of such precursor gases requires processing at relatively high temperatures; *i.e.* higher than 600°C, and generally between 600°C and 900°C because of the high

thermal stability of hydrochlorosilanes. The need to employ such high temperatures not only adds heating costs in the method of depositing such layers, but can be detrimental to the target wafer.

Therefore, there remains a need in the art for improvements in the field of selective epitaxial growth of silicon germanium semiconductor layers.

Summary of the Invention

The present invention overcomes the problems associated with SiGe layer deposition that occur in the prior art. In particular, the present invention provides a method and means for low temperature selective epitaxy of SiGe layers on semiconductor substrates. The low thermal budget processes of the present invention used in depositing selective SiGe layers improves device performance and reduces production cost.

Detailed Description of the Invention

In accordance with the present invention, by using different source gases for the epitaxial growth, it is possible to grow SiGe layers at significantly lower temperatures than those employed in the prior art.

The present invention utilizes halogermanes and silanes as the source gases in order to grow the SiGe layers at temperatures below 600°C. These gases replace the chlorosilanes and germanes of the prior art. In accordance with the present invention, SiGe layers are deposited using halogermanes and silanes as the precursor materials in accordance with the following chemical reaction equation.

$$GeH_2Cl_2 + SiH_4 \longrightarrow SiGe + 2HCl + 2H_2$$

The deposition temperature for the above reaction is considerably lower than that required in the prior art as will be shown in the examples below.

The halogermanes that can be utilized in the present invention include, but are not limited to, those having the following formula.

$X_{4-n}GeH_n$, where X is F, Cl, Br, or I, and n is 0 to 3.

Specific examples that meet the above formula include chlorogermane, dichlorogermane, and trichlorogermane.

In addition, halogermanes that can be used in the present invention include halodigermanes of the formula

$X_{3-m}H_mGeGeH_nX_{3-n}$, where X is F, Cl, Br, or I, m is 0 to 3 and n is 0 to 3;

organogermanes of the formula

$R_{4-n}GeH_n$, where R is a hydrocarbon group, and n is 0 to 3; and

organogermanium halides of the formula

$R_{4-n}GeX_n$, where R is a hydrocarbon group, X is F, Cl, Br, or I, and n is 1 to 3.

The method and means of the present invention also includes the optional addition of a further chlorine source, such as Cl_2 or HCl.

Silanes that are useful in the method and means of the present invention include, but are not limited to, silane (SiH_4), disilane (Si_2H_6), trisilane (Si_3H_8), other higher order silanes, and organosilanes of the formula

$R_{4-n}SiH_n$, where R is a hydrocarbon group, and n is 0 to 3.

The present invention is also applicable to the selective epitaxial growth of SiGeC layers, for which a source of carbon must also be provided. In particular, the present invention can utilize any suitable carbon source, such as monomethylsilane (CH_3SiH_3) and other organosilanes.

Because the halogermanes used in the present invention have a lower decomposition temperature than the hydrochlorosilanes of the prior art, the epitaxial deposition can be carried out at lower temperatures than those necessary for the prior art methods. In particular, the method and means of the present invention operates in a temperature range of 100°C to 1000°C, preferably 400°C to 600°C.

One advantage of the present invention is that the same selective epitaxial growth achieved by prior art methods, can still be accomplished, using the same hardware configurations. Therefore, no addition capital cost will be incurred and because the heating requirements are less, lower process costs may be realized. Further, the lower temperatures needed in accordance with the present invention reduce the risk of damage to under-layer and dopant profiles of the target wafers.

In this light, standard epitaxial growth chambers can be used, such as the AMAT Epi Centura and Epsilon 2000 ASM CVD systems. These chambers may be configured and set up to operate in conjunction with cleaning chambers, capping layer deposition chambers, etc. The present invention is applicable to any standard epitaxial growth process, including ultra-high vacuum CVD (UHV-CVD), low-pressure CVD (LPCVD), reduced-pressure CVD (RPCVD), rapid thermal CVD (RTCVD), and molecular beam epitaxy (MBE) processes.

Further, the SiGe or SiGeC layers of the present invention may be grown on crystalline substrates, such as single crystalline silicon substrates, a silicon layer formed on an insulator (SOI) substrate or layer, or selectively grown on silicon surfaces exposed through an amorphous surface such as a mask of SiO_2 or Si_3N_4,.

The following examples are provided to show results achieved by the method and means of the present invention, but are not intended to limit the scope of the present invention.

Example 1

A CVD chamber is baked and pumped down to base pressure below 10^{-6} Torr. Dichlorogermane (GeH_2Cl_2) and silane (SiH_4) are then delivered to the CVD chamber at a continuous rate between 1 sccm and 1000 sccm. A masked silicon wafer substrate present in the CVD chamber is heated to a temperature between 100°C to 1000°C, preferred 400°C to 600°C and the CVD chamber pressure is held between 1 mTorr and 10 Torr. An epitaxial $Si_{1-x}Ge_x$ (x = 0 to 0.5) was selectively grown on exposed portions of the silicon wafer surface.

Example 2

In a similar process as described in example 1, a carbon source such a methylsilane or hydrocarbon, is also delivered to the CVD chamber. An epitaxial layer of $Si_{1-x-y}Ge_xC_y$ (x = 0 to 0.5, y = 0 to 0.3) was selectively grown on exposed portions of the silicon wafer surface.

Example 3

In a similar process as described in example 1, a relaxed and graded layer of $Si_{1-x}Ge_x$ (x = 0 to 0.5) was selectively grown on exposed portions of the silicon wafer surface. A strained silicon layer is then deposited on the relaxed $Si_{1-x}Ge_x$ surface.

It is anticipated that other embodiments and variations of the present invention will become readily apparent to the skilled artisan in the light of the foregoing description and examples, and it is intended that such embodiments and variations likewise be included within the scope of the invention as set out in the appended claims.

CLAIMS

1. A method for forming a SiGe layer on a semiconductor substrate, said method comprising:

providing a deposition chamber having said semiconductor substrate located therein;

introducing a halogermane precursor gas as a source material for germanium to said chamber;

introducing a silane precursor gas as a source material for silicon to said chamber;

reacting said halogermane precursor and said silane precursor to create SiGe;

depositing said SiGe on to said semiconductor substrate.

2. A method according to claim 1, wherein said step of reacting is carried out in a temperature range of 100°C to 1000°C.

3. A method according to claim 2, wherein said temperature range is 400°C to 600°C.

4. A method according to claim 1, wherein said step of reacting is carried out at a temperature below 600°C.

5. A method according to claim 1, wherein said halogermane is a halogermane according to the formula $X_{4-n}GeH_n$, where X is F, Cl, Br, or I, and n is 0 to 3; a halodigermane according to the formula $X_{3-m}H_mGeGeH_nX_{3-n}$, where X is F, Cl, Br, or I, m is 0 to 3 and n is 0 to 3; an organogermane according to the formula $R_{4-n}GeH_n$, where R is a hydrocarbon group, and n is 0 to 3; or an organogermanium halide according to the formula $R_{4-n}GeX_n$, where R is a hydrocarbon group, X is F, Cl, Br, or I, and n is 1 to 3.

6. A method according to claim 1, wherein said halogermane is selected from the group consisting of chlorogermane, dichlorogermane, and trichlorogermane.

7. A method according to claim 1, further including the step of introducing Cl_2 or HCl as a source of chlorine to said chamber.

8. A method according to claim 1, wherein said silane is selected from the group consisting of silane, disilane, trisilane, other higher order silanes, and organosilanes according to the formula $R_{4-n}SiH_n$, where R is a hydrocarbon group, and n is 0 to 3.

9. A method according to claim 1, wherein said steps of reacting and depositing comprises an epitaxial growth process selected from the group consisting of ultra-high vacuum CVD, low-pressure CVD, reduced-pressure CVD, rapid thermal CVD, and molecular beam epitaxy.

10. A method according to claim 1, wherein said halogermane and said silane are introduced to said chamber at a continuous rate between 1 sccm and 1000 sccm.

11. A method according to claim 1, wherein said chamber pressure is held between 1 mTorr and 10 Torr.

12. A method according to claim 1, wherein said semiconductor substrate is a silicon wafer, a silicon layer on an insulator (SOI) substrate, or a silicon surface exposed through a mask.

13. A method according to claim 1, wherein said SiGe layer comprises $Si_{1-x}Ge_x$ where x is 0 to 0.5.

14. A method according to claim 1, wherein said SiGe layer is selected from the group consisting of a relaxed layer, a graded layer, a strained layer or combinations thereof.

15. A method according to claim 1, wherein said SiGe layer is a SiGeC layer and the method further comprises:

introducing a carbon precursor gas as a source material for carbon to said chamber;

reacting said halogermane precursor, said silane precursor and said carbon precursor to create SiGeC;

depositing said SiGeC on to said semiconductor substrate.

16. A method according to claim 15, wherein said carbon precursor is selected from the group consisting of a hydrocarbon and monomethylsilane or other organosilanes.

17. A method according to claim 15, wherein said SiGeC layer comprises $Si_{1-x-y}Ge_xC_y$ where x is 0 to 0.5 and y is 0 to 0.3.

18. A SiGe layer resulting from the reaction of a halogermane and a silane.

19. A layer according to claim 18, further including carbon from a carbon precursor.

20. A layer according to claim 18 wherein said layer is formed at a reaction temperature lower than 600°C.

21. A layer according to claim 19 wherein said layer is formed at a reaction temperature lower than 600°C.