WHAT IS CLAIMED IS:

1. A non-volatile memory device comprising:

a memory cell region including an upper substrate, channel structures, and a first upper metal line, the channel structure extending in a vertical direction on the upper substrate, the first upper metal line extending in a first horizontal direction above the channel structures; and

a peripheral circuit region below the memory cell region in the vertical direction, the peripheral circuit region including a first lower metal line extending in a second horizontal direction, a first via structure on the first lower metal line, and a second via structure on the first lower metal line, a top surface of the second via structure being in contact with the upper substrate,

wherein the memory cell region further includes a first through-hole via structure, the first through-hole via structure extending in the vertical direction, passing through the upper substrate and the first via structure, and electrically connecting the first upper metal line to the first lower metal line, and

wherein the first upper metal line is electrically connected to the upper substrate through the first through-hole via structure, the first lower metal line, and the second via structure.

2. The non-volatile memory device of claim 1, wherein the upper substrate includes a plate common source line.

3. The non-volatile memory device of claim 1 or claim 2, wherein the first upper metal line corresponds to a common source line tapping wire.

4. The non-volatile memory device of any one of claims 1 to 3, wherein the first horizontal direction is perpendicular to the second horizontal direction.

5. The non-volatile memory device of any one of claims 1 to 4, wherein the memory cell region further includes:

a plurality of bit lines at a same level in the vertical direction as the first upper metal line and extending in the first horizontal direction; and

bit line through-hole via structures in a bit line through-hole via region extending in the second horizontal direction, the bit line through-hole via structures respectively electrically connecting the plurality of bit lines to the peripheral circuit region.

6. The non-volatile memory device of any one of claims 1 to 5, wherein the first through-hole via structure is adjacent to a word line cut structure in the first horizontal direction, and

the peripheral circuit region further includes a control logic circuit below the word line cut structure and the first through-hole via structure in the vertical direction.

7. The non-volatile memory device of any one of claims 1 to 5, wherein the first through-hole via structure is between a top edge of the upper substrate and a word line cut structure adjacent to the top edge of the upper substrate.

8. The non-volatile memory device of any one of claims 1 to 5, wherein the first through-hole via structure is between a bottom edge of the upper substrate and a word line cut structure adjacent to the bottom edge of the upper substrate.

9. The non-volatile memory device of claim 1, wherein the upper substrate includes polysilicon including an impurity-doped region, and

the impurity-doped region corresponds to a plate common source line.

10. The non-volatile memory device of claim 1, wherein the upper substrate includes a polysilicon, a first conductive plate, and a second conductive plate that are sequentially stacked, and

the first and second conductive plates correspond to a plate common source line.

11. A non-volatile memory device comprising:

a first semiconductor layer including a plate common source line, channel structures, a common source line tapping wire, and a first through-hole via structure, the channel structures extending in a vertical direction on the plate common source line, the common source line tapping wire extending in a first horizontal direction on the channel structures, the first through-hole via structure passing through the plate common source line and extending in the vertical direction; and

a second semiconductor layer below the first semiconductor layer in the vertical direction, the second semiconductor layer including a lower substrate, circuit elements on the lower substrate, a plurality of lower metal layers connected to the circuit elements, and a plurality of via structures on a first lower metal layer adjacent to the first semiconductor layer among the plurality of lower metal layers, the first lower metal layer extending in a second horizontal direction,

wherein the first through-hole via structure electrically connects the common source line tapping wire to the first lower metal layer, and

the common source line tapping wire is electrically connected to the plate common source line through the first through-hole via structure, the first lower metal layer, and the plurality of via structures.

12. The non-volatile memory device of claim 11, wherein the first semiconductor layer further includes:

a plurality of bit lines at a same level in the vertical direction as the common source line tapping wire and extending in the first horizontal direction; and

bit line through-hole via structures in a bit line through-hole via region extending in the second horizontal direction, the bit line through-hole via structures respectively electrically connecting the plurality of bit lines to a peripheral circuit region.

13. The non-volatile memory device of claim 12, wherein the second semiconductor layer further includes a page buffer below the bit line through-hole via region in the vertical direction, and

the bit line through-hole via structures electrically connect the plurality of bit lines to the page buffer.

14. The non-volatile memory device of claim 12 or claim 13, wherein the first through-hole via structure is adjacent to the bit line through-hole via region in the first horizontal direction.

15. The non-volatile memory device of any one of claims 11 to 14, wherein the first through-hole via structure is adjacent to a word line cut structure in the first horizontal direction, and

the second semiconductor layer further includes a control logic circuit below the word line cut structure and the first through-hole via structure in the vertical direction.

16. A non-volatile memory device comprising:

a first semiconductor layer including a first memory block, a second memory block, a first through-hole via region adjacent to the first memory block, a bit line through-hole via region adjacent to the first through-hole via region, and a second through-hole via region between the bit line through-hole via region and the second memory block; and

a second semiconductor layer below the first semiconductor layer in a vertical direction, the second semiconductor layer including a first lower metal line and a second lower metal line separated from the first lower metal line in a first horizontal direction,

wherein the first through-hole via region includes a first through-hole via structure connecting a first upper metal line to the first lower metal line, the first upper metal line being above the first and second memory blocks and extending in the first horizontal direction,

the second through-hole via region includes a second through-hole via structure connecting the first upper metal line to the second lower metal line,

the first semiconductor layer further includes a plate common source line,

the second semiconductor layer further includes a first via structure on the first lower metal line and a second via structure on the second lower metal line,

the first upper metal line is electrically connected to the plate common source line through the first through-hole via structure, the first lower metal line, and the first via structure, and

the first upper metal line is electrically connected to the plate common source line through the second through-hole via structure, the second lower metal line, and the second via structure.

17. The non-volatile memory device of claim 16, wherein the first semiconductor layer further includes a plurality of bit lines at a same level in the vertical direction as the first upper metal line, and

the bit line through-hole via region includes bit line through-hole via structures connecting the plurality of bit lines to the second semiconductor layer.

18. The non-volatile memory device of claim 17, wherein each of the first and second memory blocks includes channel structures extending in the vertical direction and connected to the plurality of bit lines.

19. The non-volatile memory device of any one of claims 16 to 18, wherein the first and second lower metal lines are at a same level in the vertical direction as each other and extend in a second horizontal direction that is perpendicular to the first horizontal direction.