CLAIMS

1. A substrate comprising:

a first portion of the substrate including a first plurality of metal layers,

wherein the first plurality of metal layers includes a first plurality of interconnects located on a first surface of the first portion of the substrate, and

wherein the first plurality of interconnects are part of a metal layer located on the first surface of the first portion of the substrate;

a second portion of the substrate including a second plurality of metal layers,

wherein the second plurality of metal layers includes a second plurality of interconnects located on a second surface of the second portion of the substrate, and

wherein the second plurality of interconnects are part of another metal layer located on the second surface of the second portion of the substrate;

a plurality of insulating layers configured to separate metal layers within the first plurality of metal layers and metal layers within the second plurality of metal layers;

a first plurality of pads located on the first metal layer, and a second plurality of pads located on the second metal layer;

a first plurality of posts located on the first plurality of pads and a plurality of solder interconnects located on the second plurality of pads coupled together such that (i) the first plurality of posts and the plurality of solder interconnects couple the first portion of the substrate to the second portion of the substrate, and (ii) the first surface of the first portion of the substrate faces the second surface of the second portion of the substrate; and

a mold located in a gap between the first plurality of pads and between the first plurality of posts.

2. The substrate of claim 1, further comprising:

a first metal layer of the first plurality of metal layers, wherein the first metal layer includes a first plurality of traces embedded in the first portion of the substrate; and

a second metal layer of the second plurality of metal layers, wherein the second metal layer includes a second plurality of traces embedded in the second portion of the substrate.

3. The substrate of claim 2:

wherein the first metal layer is a top layer of the substrate, and the first plurality of traces are configured to couple to a surface mount circuit component; and

wherein the second metal layer is a bottom layer of the substrate, and the second plurality of traces are configured to couple to another surface mount circuit component.

4. The substrate of claim 2:

wherein the first plurality of posts are located on an inner metal layer of the substrate; and

wherein the substrate further comprises a second plurality of posts that are located on another inner metal layer of the substrate.

5. The substrate of claim 1,

wherein the first plurality of interconnects and the second plurality of interconnects are encapsulated by the mold, and

wherein the mold includes a non-conductive paste and/or a non-conductive film.

6. The substrate of claim 1,

wherein the plurality of solder interconnects are located inside of the substrate, and

wherein the plurality of solder interconnects are located between the first portion of the substrate and the second portion of the substrate.

7. The substrate of claim 6, wherein the plurality of solder interconnects are at least partially surrounded by photoresist.

8. The substrate of claim 1,

wherein the first plurality of metal layers from the first portion of the substrate includes three or more metal layers, and

wherein the second plurality of metal layers from the second portion of the substrate includes three or more metal layers.

9. The substrate of claim 1, wherein the substrate is incorporated into a device selected from a group consisting of a music player, a video player, an entertainment unit, a navigation device, a

communications device, a mobile device, a mobile phone, a smartphone, a personal digital assistant, a fixed location terminal, a tablet computer, a computer, a wearable device, a laptop computer, a server, an internet of things (IoT) device, and a device in an automotive vehicle.

10. A method of fabricating a substrate, comprising:

forming a first portion of the substrate including forming a first plurality of metal layers comprising a metal layer that is located on a first surface of the first portion of the substrate;

forming a second portion of the substrate including forming a second plurality of metal layers comprising another metal layer that is located on a second surface of the second portion of the substrate;

forming a plurality of insulating layers configured to separate metal layers within the first plurality of metal layers and metal layers within the second plurality of metal layers;

forming a first plurality of pads located on the first metal layer, and a second plurality of pads located on the second metal layer;

forming a first plurality of posts located on the first plurality of pads and a plurality of solder interconnects located on the second plurality of pads;

coupling the first plurality of posts to the plurality of solder interconnects such that (i) the first portion of the substrate and the second portion of the substrate are coupled together, and (ii) the first surface of the first portion of the substrate faces the second surface of the second portion of the substrate, wherein coupling the first plurality of posts to the plurality of solder interconnects forms a gap between the first portion of the substrate and the second portion of the substrate; and

after coupling the first plurality of posts to the plurality of solder interconnects, filling the gap with a mold, such that the mold fills a gap between the first plurality of pads and between the first plurality of posts .

11. The method of claim 10, further comprising:

forming a first plurality of traces embedded in the first portion of the substrate, the first plurality of traces formed in a first metal layer of the first plurality of metal layers; and

forming a second plurality of traces embedded in the second portion of the substrate, the second plurality of traces formed in a second metal layer of the second plurality of metal layers.

12. The method of claim 11:

wherein the first metal layer is a top layer of the substrate, and the first plurality of traces are configured to couple to a surface mount circuit component; and

wherein the second metal layer is a bottom layer of the substrate, and the second plurality of traces are configured to couple to another surface mount circuit component.

13. The method of claim 10, wherein the mold includes a non-conductive paste and/or a non-conductive film.

14. The method of claim 10, wherein the plurality of solder interconnects are located inside of the substrate.

15. The method of claim 14, wherein the plurality of solder interconnects are at least partially surrounded by photoresist.