A METHOD TO FORM MOS TRANSISTORS WITH SHALLOW JUNCTIONS USING LASER ANNEALING

ABSTRACT

A new method of forming MOS transistors with shallow source and drain extensions and self-aligned silicide in the has been achieved. Gates are provided overlying a semiconductor substrate. Temporary sidewall spacers are formed on the gates. Ions are implanted into the semiconductor substrate and the polysilicon layer to form deep amorphous layers beside the spacers and shallow amorphous layers under the spacers. The spacers are removed. Ions are implanted to form lightly doped junctions in the shallower amorphous layer. Permanent sidewall spacers are formed on the gates. Ions are implanted to form heavily doped junctions in the deeper amorphous layer. A metal layer is deposited. A capping layer is deposited to protect the metal layer during irradiation. The integrated circuit device is irradiated with laser light to melt the amorphous layer while the crystalline polysilicon and semiconductor substrate remain in solid state. The metal layer is heated, and may be melted, to cause reaction with the silicon to form silicide. Ions in the heavily doped junctions and in the lightly doped junctions are also thereby diffused into the amorphous layer. The deep source and drain junctions, the shallow source and drain extensions, and a silicide layer are simultaneously formed. A heat treatment crystallizes the silicide to improve resistivity.

Figure 4