CLAIMS

1. A quantum computing device, comprising:

a device region located on a superconductor layer above a semiconductor layer;

a first nanorod region and a second nanorod region located within the device region, wherein the second nanorod region is substantially parallel to the first nanorod region, wherein the first nanorod region and the second nanorod region are configured with dimensions appropriate to act as a one-dimensional topological superconductor;

a sensing region located within the device region, the sensing region comprising a portion of the device region including no superconductor layer, wherein the sensing region comprises a quantum dot, the sensing region connecting the first nanorod region and the second nanorod region;

a tunnel junction gate comprising a first metal within the sensing region;

a chemical potential gate comprising a dielectric and the first metal within a portion of the device region outside the sensing region;

a sensing region gate comprising a second metal coupled to the semiconductor layer within the sensing region; and

a nanorod contact comprising the second metal coupled to the superconductor layer within the portion of the device region outside the sensing region.

2. The quantum computing device of claim 1, further comprising:

a buffer layer formed on a first surface of a substrate;

a first protective layer formed on the buffer layer; and

the semiconductor layer formed on the first protective layer

3. The quantum computing device of claim 2, wherein the buffer layer comprises indium aluminum arsenide.

4. The quantum computing device of any one of claims 2 to 3, wherein the first protective layer comprises indium gallium arsenide.

5. The quantum computing device of any one of the preceding claims, wherein the superconductor layer comprises aluminum.

6. The quantum computing device of any one of the preceding claims, further comprising:

a second protective layer formed between the semiconductor layer and the superconductor layer.

7. The quantum computing device of any one of the preceding claims, further comprising:

an isolation region surrounding the device region, the isolation region comprising a region in which the superconductor layer has been removed and the semiconductor layer implanted.

8. A computer-implemented method to fabricate a quantum computing device, the method comprising:

forming, on a superconductor layer, a first resist pattern defining a device region and a sensing region within the device region, wherein the device region comprises a first nanorod region, a second nanorod region substantially parallel to the first nanorod region, and the sensing region connecting the first nanorod region and the second nanorod region; wherein the first nanorod region and the second nanorod region are dimensioned appropriately to act as a one-dimensional topological superconductor; wherein the sensing region comprises a quantum dot;

removing, using an etching process, the superconductor layer within the sensing region, the etching exposing a region of an underlying semiconductor layer outside the device region unprotected by the first resist pattern;

implanting the exposed region of the semiconductor layer, the implanting forming an isolation region surrounding the device region;

exposing, using an etching process subsequent to the implanting, the sensing region and a portion of the device region of the superconductor layer adjacent to the isolation region;

forming, by depositing a first metal layer within the sensing region, a tunnel junction gate;

forming, by depositing a dielectric layer and the first metal layer within the portion of the device region outside the sensing region, a chemical potential gate;

forming a sensing region gate by coupling the semiconductor layer with a second metal layer; and

forming a nanorod contact using the second metal within the portion of the device region outside the sensing region.

9. The computer-implemented method of claim 8, further comprising:

forming, on a first surface of a substrate, a buffer layer;

forming, on the buffer layer, a first protective layer;

forming, on a first protective layer, the semiconductor layer; and

forming, on the semiconductor layer, the superconductor layer.

10. The computer-implemented method of claim 9, wherein the buffer layer comprises indium aluminum arsenide.

11. The computer-implemented method of any one of claims 9 to 10, wherein the first protective layer comprises indium gallium arsenide.

12. The computer-implemented method of any one of claims 8 to 11, wherein the superconductor layer comprises aluminum.

13. The computer-implemented method of any one of claims 8 to 12, further comprising:

forming, between the semiconductor layer and the superconductor layer, a second protective layer.

14. The computer-implemented method of any one of claims 8 to 13, further comprising:

removing, prior to depositing the first metal layer, the first resist pattern.

15. The computer-implemented method of any one of claims 8 to 14, wherein depositing the first metal layer is performed in regions defined by a second resist pattern.

16. The computer-implemented method of any one of claims 8 to 15, wherein the second metal layer is formed by depositing the second metal layer in regions defined by a third resist pattern, the third resist pattern protecting the tunnel junction gate and the chemical potential gate.

17. A superconductor fabrication system comprising a lithography component, the superconductor fabrication system when operated on at least one die to fabricate a quantum computing device performing operations comprising:

forming, on a superconductor layer, a first resist pattern defining a device region and a sensing region within the device region, wherein the device region comprises a first nanorod region, a second nanorod region substantially parallel to the first nanorod region, and the sensing region connecting the first nanorod region and the second nanorod region; wherein the first nanorod region and the second nanorod region are dimensioned appropriately to act as a one-dimensional topological superconductor; wherein the sensing region comprises a quantum dot;

removing, using an etching process, the superconductor layer within the sensing region, the etching exposing a region of an underlying semiconductor layer outside the device region unprotected by the first resist pattern;

implanting the exposed region of the semiconductor layer, the implanting forming an isolation region surrounding the device region;

exposing, using an etching process subsequent to the implanting, the sensing region and a portion of the device region of the superconductor layer adjacent to the isolation region;

forming, by depositing a first metal layer within the sensing region, a tunnel junction gate;

forming, by depositing a dielectric layer and the first metal layer within the portion of the device region outside the sensing region, a chemical potential gate;

forming a sensing region gate by coupling the semiconductor layer with a second metal layer; and

forming a nanorod contact using the second metal within the portion of the device region outside the sensing region.