WHAT IS CLAIMED IS:

1. A semiconductor memory device, comprising:

a peripheral logic structure including peripheral circuits on a substrate;

a horizontal semiconductor layer extending along a top surface of the peripheral logic structure;

a plurality of stack structures arranged on the horizontal semiconductor layer along a first direction; and

a plurality of electrode separation regions in each of the plurality of stack structures to extend in a second direction, which is different from the first direction,

wherein each of the plurality of stack structures includes a first electrode pad and a second electrode pad on the first electrode pad, the first electrode pad protruding in the first direction beyond the second electrode pad by a first width, and the first electrode pad protrudes in the second direction beyond the second electrode pad by a second width, which is different from the first width,

wherein the first electrode pad comprises a first electrode region and a first mold region which extends in the first direction from the first electrode region, and

wherein the second electrode pad comprises a second electrode region and a second mold region which extends in the second direction from the second electrode region.

2. The semiconductor memory device as claimed in claim 1, wherein the second width is greater than the first width.

3. The semiconductor memory device as claimed in claim 1, wherein a width, in the first direction, of the first mold region of the first electrode pad is greater than a width, in the first direction, of the second mold region of the second electrode pad.

4. The semiconductor memory device as claimed in claim 1, wherein the first mold region of the first electrode pad protrudes in the first direction beyond the second mold region of the second electrode pad by the first width.

5. The semiconductor memory device as claimed in any one of claims 1 to 4, wherein the plurality of stack structures includes:

first and second stack structures which are adjacent to each other along the first direction, and

a plurality of through electrodes between the first and second stack structures.

6. The semiconductor memory device as claimed in claim 5, wherein the plurality of through electrodes do not penetrate the first and second stack structures.

7. The semiconductor memory device as claimed in claim 5, wherein some of the plurality of through electrodes penetrate at least one of the first and second stack structures.

8. The semiconductor memory device as claimed in any one of claims 5 to 7, wherein:

the horizontal semiconductor layer includes openings which expose parts of the peripheral logic structure, and

the plurality of through electrodes are electrically connected to the peripheral circuits through the openings.

9. The semiconductor memory device as claimed in claim 1, further comprising a third electrode pad on the second electrode pad and the first electrode pad, wherein:

the third electrode pad is at a top of each of the plurality of stack structures, and

the third electrode pad includes a third electrode region and does not include a third mold region.

10. The semiconductor memory device as claimed in claim 1, wherein the first and second electrode regions are on both sides of the first and second mold regions, and extend in the first direction.

11. The semiconductor memory device as claimed in claim 10, further comprising:

at least one through electrode penetrating the first and second mold regions of the first and second electrode pads,

wherein the horizontal semiconductor layer includes openings which expose parts of the peripheral logic structure, and

wherein the at least one through electrode is electrically connected to the peripheral circuits through the openings.

12. The semiconductor memory device as claimed in any one of claims 1 to 11, wherein:

each of the plurality of stack structures includes a plurality of electrode separation trenches, and

the plurality of electrode separation regions includes an insulating material that fills the plurality of electrode separation trenches.

13. A semiconductor memory device, comprising:

a peripheral logic structure including first peripheral circuits and second peripheral circuits on a substrate;

first and second stack structures arranged on the peripheral logic structure along a first direction;

a plurality of electrode separation regions in the first stack structure to extend in a second direction, which is different from the first direction;

a plurality of first through electrodes arranged between the first and second stack structures along the first direction to be electrically connected to the first peripheral circuits, at least one of the plurality of first through electrodes not penetrating the first and second stack structures; and

a plurality of second through electrodes electrically connected to the second peripheral circuits through the first stack structure and arranged along the second direction, wherein:

the first stack structure includes a first electrode pad and a second electrode pad on the first electrode pad,

the first electrode pad comprising a first electrode region and a first mold region which extends in the first direction from the first electrode region, and

the second electrode pad comprising a second electrode region and a second mold region which extends in the second direction from the second electrode region.

14. The semiconductor memory device as claimed in claim 13, wherein the plurality of first through electrodes does not penetrate the first and second stack structures.

15. The semiconductor memory device as claimed in claim 13 or claim 14, wherein:

the first electrode pad protrudes in the first direction beyond the second electrode pad by a first width, and

the first electrode pad protrudes in the second direction beyond the second electrode pad by a second width, which is different from the first width.

16. The semiconductor memory device as claimed in claim 13 or claim 14, wherein:

the first and second electrode pads of the first stack structure are sequentially stacked on the peripheral logic structure,

the plurality of electrode separation regions includes first and second electrode separation regions which are the most apart from each other in the first direction, each of the first and second electrode pads include the first and second electrode region which is between the first and second electrode separation regions, and

the first stack structure has a stepped profile defined by the first and second mold regions of the first and second electrode pads.

17. The semiconductor memory device as claimed in claim 13 or claim 14, wherein:

the first and second electrode pads of the first stack structure are sequentially stacked on the peripheral logic structure, and

the plurality of second through electrodes penetrate at least one of the first and the second mold regions.

18. A semiconductor memory device, comprising:

a peripheral logic structure including first peripheral circuits and second peripheral circuits on a substrate;

a horizontal semiconductor layer on the peripheral logic structure, the horizontal semiconductor layer including a plurality of openings which extend in a first direction;

first and second stack structures on the horizontal semiconductor layer and arranged in a second direction with one of the plurality of openings therebetween;

a plurality of electrode separation regions in the first stack structure to extend in the first direction;

a plurality of vertical structures between the plurality of electrode separation regions, which are adjacent to one another, to penetrate the first stack structure and to be electrically connected to the horizontal semiconductor layer;

bitlines on the first stack structure to extend in the second direction and to be connected to at least one of the plurality of vertical structures;

a plurality of first through electrodes penetrating the plurality of openings and connecting the bitlines and the first peripheral circuits; and

a plurality of second through electrodes electrically connected to the second peripheral circuits through the first stack structure, wherein:

the first stack structure includes a first electrode pad and a second electrode pad on the first electrode pad,

the first electrode pad comprising a first electrode region and a first mold region which extends in the first direction from the first electrode region, and

the second electrode pad comprising a second electrode region and a second mold region which extends in the second direction from the second electrode region.

19. The semiconductor memory device as claimed in claim 18, wherein:

the first electrode pad protrudes in the first direction beyond the second electrode pad by a first width, and

the first electrode pad protrudes in the second direction beyond the second electrode pad by a second width, which is different from the first width.