METHOD OF FABRICATING A SPLIT GATE MEMORY CELL

Abstract

A method of fabricating a novel split gate memory cell comprises forming a tunnel oxide layer on a silicon substrate, forming a first conductive layer over said tunnel oxide layer, etching a trench in said conductive layer to divide said conductive layer into two separate layers with a space therebetween, one such layer to become a first gate electrode and the other separate layer to become a floating gate electrode of the device, forming a dielectric layer over the exposed surfaces, and depositing a second conductive layer which will become a second control gate electrode over said dielectric layer.

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