

CLAIMS**1.** An amplifier circuit which includes:

a resistor divider (R_{REF}) comprising n resistive elements (r_n) in series where $n > 1$, wherein:

5 the resistor divider (R_{REF}) comprises two main nodes defined at each end thereof, namely a first main node (a) and a second main node (b);

 the resistor divider (R_{REF}) also comprises two readout nodes (d_1 , d_2), namely a first readout node (d_1) and a second readout node (d_2);

10 the resistor divider (R_{REF}) comprises resistor nodes (q) defined between adjacent resistive elements;

 an input current source (I_{REF}) is connected to the first main node (a);

 the resistor divider (R_{REF}) comprises two arrays of addressable switch elements, with a first array of switch elements provided between the respective resistive nodes (q) of the resistive elements and the first readout node (d_1) and with a second array of switch elements provided between the respective resistive nodes (q) of the resistive elements and the second readout node (d_2); and

20 a state of the switch elements is controlled by a feedback signal (S_{FB}) to be open or closed, the resistive elements thus acting as selectable voltage taps with connected the readout nodes (d_1 , d_2);

 a differential pair of transistors (T_1 , T_2) comprising a first transistor (T_1) having at least four terminals and a second transistor (T_2) having at least four terminals, wherein:

25 source terminals of each of the transistors (T_1 , T_2) are connected to the second node (b);

 gate terminals of the transistors (T_1 , T_2) are connected to respective input signals (v_1 , v_2);

30 drain terminals of the transistors (T_1 , T_2) are connected to respective current sources (I_1 , I_2), wherein a differential output signal (v_{OUT}) is created between the drain terminals of the transistors (T_1 , T_2); and

bulk terminals of the transistors (T_1 , T_2) are connected to the respective readout nodes (d_1 , d_2);

wherein the amplifier circuit is configured to perform a function of a difference amplifier in that the transistors (T_1 , T_2) form a differential amplifier with
5 respective input signals (v_1 , v_2) on their gate terminals; and

wherein the bulk terminals affect a threshold of the respective transistors (T_1 , T_2) so as to add or subtract a differential signal derived from the readout nodes (d_1 , d_2) of the resistor divider (R_{REF}) based on voltage signals generated by the operation of the resistor divider (R_{REF}) determined by the feedback signal
10 (S_{FB}).

2. The amplifier circuit as claimed in claim 1, in which the input signals (v_1 , v_2) are derived from an external source in the form of a sensor.

15 3. The amplifier circuit as claimed in any one of claims 1-2, in which the transistors (T_1 , T_2) are MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors).

4. The amplifier circuit as claimed in any one of claims 1-3, in which the readout nodes (d_1 , d_2) are differential nodes and the signals at the readout nodes (d_1 , d_2) are a
20 differential representation of the feedback signal (S_{FB}).

5. The amplifier circuit as claimed in any one of claims 1-4, which is configured to perform a function of an integrator where the differential pair formed by the transistors (T_1 , T_2), the current sources (I_1 , I_2), nodal parasitic capacitances and resistances
25 present on nodes connected to the drain terminals of the respective transistors (T_1 , T_2), and the operation of the amplifier circuit as a differential difference amplifier with respect to differential signals (v_1 , v_2) and (d_1 , d_2) causes the differential output (V_{OUT}) to exhibit characteristics of an integrated output.

6. The amplifier circuit as claimed in claim 5, in which capacitors are added to the nodes connected to the drain terminals of the respective transistors (T_1 , T_2) to alter integrator action.

5 **7.** The amplifier circuit as claimed in claim 6, in which feedback in the form of the feedback signal (S_{FB}) is applied directly to the transistors (T_1 , T_2), effectively creating a differential amplifier for direct application in sigma-delta converters.

10 **8.** The amplifier circuit as claimed in any one of claims 1-7, which is configured to receive the respective input signals (v_1 , v_2):

differential signals; or

a variable input signal and a fixed or ground input signal.

15 **9.** The amplifier circuit as claimed in any one of claims 1-8, which is, or which forms part of, an integrated circuit.

10. A sigma-delta analogue-to-digital converter which includes the amplifier circuit as claimed in any one of claims 1-9.

20 **11.** The sigma-delta analogue-to-digital converter as claimed in claim 10, which includes a summation node and in which the transistors (T_1 , T_2) are configured to function as, or forms part of, the summation node.

25 **12.** The sigma-delta analogue-to-digital converter as claimed in any one of claims 10-11, which includes a DAC (Digital-to-Analogue Converter) and in which the resistor divider (R_{REF}) is configured to function as, or forms part of, the DAC.

13. The sigma-delta analogue-to-digital converter as claimed in any one of claims 10-12, which includes an integrator and in which the current sources (I_1 , I_2), with supporting circuitry, are configured to function as, or forms part of, are integrator.

5 **14.** The sigma-delta analogue-to-digital converter as claimed in any one of claims 10-13, which includes a comparator and in which an input of the comparator is connected to the differential output signal (V_{OUT}) of the amplifier circuit.

10 **15.** The sigma-delta analogue-to-digital converter as claimed in claim 14, which includes ADC (Analogue-to-Digital Converter) logic and in which an input of the ADC logic is connected to an output of the comparator.

16. The sigma-delta analogue-to-digital converter as claimed in claim 15, which includes feedback logic which is connected to an output of the ADC logic and which is
15 configured to generate the feedback signal (S_{FB}).

17. The sigma-delta analogue-to-digital converter as claimed in any one of claims 10-16, which is, or which forms part of, an integrated circuit.

20 **18.** A method of operating an amplifier circuit, the method including:

providing a resistor divider (R_{REF}) comprising n resistive elements (r_n) in series where $n > 1$, wherein:

the resistor divider (R_{REF}) comprises two main nodes defined at each end thereof, namely a first main node (a) and a second main node (b);

25 the resistor divider (R_{REF}) also comprises two readout nodes (d_1 , d_2), namely a first readout node (d_1) and a second readout node (d_2);

the resistor divider (R_{REF}) comprises resistor nodes (q) defined between adjacent resistive elements;

an input current source (I_{REF}) is connected to the first main node (a);

the resistor divider (R_{REF}) comprises two arrays of addressable switch elements, with a first array of switch elements provided between the respective resistive nodes (q) of the resistive elements (r_n) and the first readout node (d_1) and with a second array of switch elements provided between the respective resistive nodes (q) of the resistive elements (r_n) and the second readout node (d_2); and

a state of the switch elements is controlled by a feedback signal (s_{FB}) to be open or closed, the resistive elements (r_n) thus acting as selectable voltage taps connected to the readout nodes (d_1 , d_2);

providing a differential pair of transistors (T_1 , T_2) comprising a first transistor (T_1) having at least four terminals and a second transistor (T_2) having at least four terminals, wherein:

source terminals of each of the transistors (T_1 , T_2) are connected to the second node (b);

gate terminals of the transistors (T_1 , T_2) are connected to respective input signals (v_1 , v_2);

drain terminals of the transistors (T_1 , T_2) are connected to respective current sources (I_1 , I_2), wherein a differential output signal (v_{OUT}) is created between the drain terminals of the transistors (T_1 , T_2); and

bulk terminals of the transistors (T_1 , T_2) are connected to the respective readout nodes (d_1 , d_2);

performing, by the amplifier circuit, a function of a difference amplifier in that the transistors (T_1 , T_2) form a differential amplifier with respective input signals (v_1 , v_2) on their gate terminals; and

affecting, by the bulk terminals of the transistors (T_1 , T_2), a transconductance of the respective transistors (T_1 , T_2) so as to add or subtract a differential signal derived from the readout nodes (d_1 , d_2) of the resistor divider (R_{REF}) based on voltage signals generated by the operation of the resistor divider (R_{REF}) determined by the feedback signal (s_{FB}).