

CONTROL METHOD, SEMICONDUCTOR MEMORY, AND ELECTRONIC DEVICE

ABSTRACT

Embodiments of the present disclosure provide a control method, a semiconductor memory, and an electronic device. An impedance control strategy for a Data Mask Pin (DM pin) in a preset test mode is provided, so that the impedance of the DM pin in the preset test mode may be defined. In addition, the relation between a control signal configured to control whether to enable the DM pin in a Double Data Rate 5 SDRAM (DDR5) and a control signal configured to control whether the DM pin is a test object in a Package Output Driver Test Mode (PODTM) is specified. The impedance of the DM pin may be tested in the preset test mode to avoid circuit processing errors.

[Fig. 1]