



AN IMPROVED LIGHT SENSOR WITH INCREASED DYNAMIC RANGE

BACKGROUND OF THE INVENTIONTechnical Field

The invention relates generally to image capture systems. More specifically, the invention is related to an improved light sensor and a method of employing the improved light sensor to capture and process image data to improve dynamic range.

Background Art

Typical digital image capture systems such as digital cameras employ a sensor, memory and processor. Sensors are manufactured using charge coupled device (CCD) or complimentary metal oxides (CMOS) semiconductor processes. A typical CMOS sensor includes a pixel array having a plurality of pixel cells arranged in rows and columns. A correlated double sampler (CDS), an amplifier, and an analog-to-digital converter are also included for every column of the pixel array. In a typical system, light intensities captured in each pixel cell of the CMOS sensor are directly transferred a respective CDS). Thereafter, the image data is provided to an amplifier for amplification. The amplified signal is provided to the analog-to-digital converter, which converts the analog signal into a digital signal. Once the image data is converted into digital form, it is often stored in a memory and/or transferred for further processing either locally within the image capture system or remotely within another image processing system, such as a computer.

An important component in the processing of the image data is to compress the data for easier transmission and/or storage. In the prior art approach, each pixel cell generates a pixel value that is first stored in memory. The stored pixel values are then manipulated and compressed by a digital signal processing (DSP) program executing on a processor.

As the size of the pixel arrays grows, the amount of local memory required to store the pixel values also increases correspondingly. For example, as the pixel array grows from 512x512 to 1024x1024 and assuming one byte per pixel, the minimal memory requirements increase from 262,144 bytes to



1,048,576 bytes for each image captured. Consequently, four times more memory is needed to store a picture.

An additional concern for video image data is the need to meet bandwidth requirements. As an array grows, additional bandwidth is needed to transfer the additional image data at a given frame rate to other image processing systems, such as computers.

As a pixel array grows from 512 x 512 to 1024 x 1024, the bandwidth required increases by approximately four times. For example, assuming 30 frames per second, the uncompressed data rate from a sensor 512 x 512 array with (1 byte) per pixel is approximately 7.8 megabytes per second for the 512 x 512 array. The data rate is increased to 31.5 megabytes per second for the 1024 x 1024 array.

To improve picture quality and to add color to a picture, typical image processing systems increase the number of bytes employed to represent each pixel. For color applications, each pixel is typically represented by more than one byte. For example, some color processing systems employ two bytes, or 16 bits, to represent a single pixel value. As each pixel is represented by a greater number of bytes, the memory requirements and bandwidth requirements increase accordingly.

In addition, for increased dynamic range in the image sensor, some current systems propose that additional memory elements be used to hold multiple readings of a single pixel such that two integration times are captured and analyzed. Consequently, it would be desirable to provide an improved sensor that would reduce the memory storage and bandwidth requirements for image capture and transmission.

SUMMARY OF THE INVENTION

In an image capture system having a sensor with a first node and a second node, a method of capturing image data is disclosed. The first node is reset. The second node is reset. An image is collected on the first node. A first pixel value is then transferred from the first node to the second node after a first predetermined time period. The first pixel value and a second pixel value is then provided after a second predetermined time period. An arithmetic operation is performed on the first pixel value and the second pixel value. A system for performing the method is also disclosed.

BRIEF DESCRIPTION OF THE DRAWINGS

The objects, features and advantages of the method and apparatus for the present invention will be apparent from the following description in which:

Figure 1 illustrates an image capture system configured in accordance with the teachings of the present invention.

Figure 2 illustrates the improved pixel cell configured in accordance with the teachings of the present invention.

Figure 3 is a simplified block diagram illustrating the pixel array and the focal plane processors of the improved sensor of the present invention.

Figure 4 is a flowchart illustrating how a signal processing program may employ the improved sensor to capture and process image data in accordance with one embodiment of the present invention.

Figure 5 is a block diagram of an image capture device (e.g., a digital camera) in which the improved sensor of the present invention may be implemented

Figure 6 is a block diagram illustrating in greater detail the digital signal processing functional block of Figure 5.

Figure 7 illustrates a computer system having a silicon eye in which the improved sensor of the present invention may be implemented.

Figure 8 is a block diagram illustrating in greater detail the computer system, shown in Figure 7.

DETAILED DESCRIPTION OF THE INVENTION

Referring to the figures, exemplary embodiments of the invention will now be described. The exemplary embodiments are provided to illustrate aspects of the invention and should not be construed as limiting the scope of the invention. The exemplary embodiments are primarily described with reference to block diagrams. Depending upon the implementation, the corresponding apparatus element may be configured in hardware, software, firmware or combinations thereof.

Figure 1 illustrates an image capture system 100 in which an improved sensor 102 of the present invention may be implemented. The improved sensor 102 interacts with a processor 140 and a memory 150 through a bus 144. In one embodiment of the present invention, the improved sensor 102 includes

a pixel array 104 having a plurality of pixels, arranged in rows and columns. For example, the pixel array 104 may include 512 x 512 pixel cells or 1024 x 1024 pixel cells. Each pixel cell features an improved architecture having a temporary storage element, a first readout circuit, and a second readout circuit, which will be described in greater detail hereinafter with reference to Figure 2.

A row selector 105 is provided to specify a particular row in the pixel array 104 based on control signals provided by the controller 110. A column selector 107 is provided to specify a column in the pixel array 104 based on control signals provided by the controller 110. The row selector 105 and the column selector 107 together specify a particular pixel cell within the pixel array 104.

The controller 110 includes one or more control registers 111 and a timing generator 112. The control registers 111 are accessible by the processor 140. For example, processor 140 may selectively read values from the registers 111 and write values into the control registers 111. The control registers 111, in turn, provide the value stored therein to the timing generator 112. The timing generator 112, based on the values provided by the control registers 111, selectively generates signals 107 to the row selector 105, the column selector 107, signals 108 to each cell in the pixel array 104, and signals 114 to a pre-processing unit 116.

The pre-processing unit 116 includes a focal plane processor 120 and an analog to digital converter 134. The focal plane processor 120 includes two inputs for receiving two pixel values 113 provided by the pixel array 104. The focal plane processor 120 performs an arithmetic or logical operation on the received values and generates a result. This result is provided to the A/D converter 134, which converts the analog result into a digital value. The digitized pixel value is then provided to bus 144 for storage or further processing. The signals 114 provided by the controller 110 to the pre-processing unit 116 specify the particular arithmetic or logical operation and also manages the timing of the processing and analog to digital conversion.

The pixel cell 106 includes an input for receiving a set of signals 108 from the controller 110 and output for providing pixel value signals 113 to the pre-processing unit 116. Control signals 108 may include, but are not limited to, RS1, RS2, Source, TX, IG, V1, and V2. These signals are described in greater detail hereinafter.

The timing generator 112 may include clock generation circuits and counters (not shown), which are known in the art. The control registers 111 may be loaded by an in-system processor 140 or indirectly by a host processor (not shown). Once loaded, the registers 111 may provide the 1) starting values, 2) increment count, 3) stopping values and 4) other information needed in the operation and control of the sequencing of the control signals.

The memory 150 may include a program 152 for providing an interface between a user and the improved sensor 102. When executing on processor 140, the program 152 may query a user for particular inputs, such as image capture time, electronic shutter controls, gain controls, light levels and specific memory types.

In the embodiment where the improved sensor 102 is incorporated in a digital camera, the program 152 may be a simple lookup table that provides hard-wired inputs to the controller 110.

In the embodiment where the image capture system 100 is tethered to a host processor (not shown), the program 152 may include graphical user interfaces (GUIs) to allow a user to interact with the improved sensor 102.

Operation of a Cell 106

The cell 106 is first selected by the row selector 105 and the column selector 107. The cell 106 includes an input for receiving the control signals 108 from the timing generator 112. In response to these control signals 108, the cell 106 generates two pixel values 113, which are provided to a pre-processing unit 116. The architecture of the improved cell 106 is described in greater detail with reference to Figure 2. The two pixel values 113 that are provided to the pre-processing unit 116 are from successive frames. The cell 106 includes a storage element for storing a first pixel value, while a second pixel value, corresponding to a pixel value in the next frame, is captured. The steps performed by the improved sensor 102 in accordance to one embodiment of the present invention is set forth in greater detail with reference to Figure 4.

It should be noted that any of cells in the pixel array 104 may be accessed in a similar fashion. In this embodiment, there is a pre-processing unit 116 associated with each column of the pixel array 104. The pre-processing units associated with the other columns of the pixel array 104 are not shown in this figure in order not to clutter the diagram.

It should be noted that, although in the preferred embodiment there is a pre-processing unit associated with each column of the pixel array 104, it is contemplated that two or more columns of the pixel array 104 may share a single pre-processing unit.

In yet another embodiment of the present invention, the pre-processing unit 116 may be integrated into each pixel cell. . In the preferred embodiment, the focal plane processor 120 may be implemented with an Arithmetic Logic Unit (ALU).

In alternative embodiments, the focal plane processor may be integrated as part of each pixel cell. Although the improved sensor 102 has been described as having a pre-processing unit 120 for each column of the pixel array 104, it will be understood that other architectures are more suitable for different applications. For example, a single pre-processing unit may receive data from two adjacent columns. In this architecture, the single pre-processing unit may compare the values of adjacent columns. Since each pixel cell includes two outputs, each pre-processing unit may receive one output from a first column and a second output from an adjacent column.

In alternative embodiments, the focal plane processor may be implemented by differencing circuits, time averaging or spatial averaging circuits. The focal plane processor may also be a compensation circuit with feedback to alter the gain of the pixel drivers, or to modify the capture characteristics of the pixel. Focal plane processor may alter the pixel data by employing the surrounding pixels or the characteristics of a single pixel. For example, the value of a pixel may be changed depending on the values of the surrounding pixels if it is so determined there needs to be compensation for the pixel.

As noted previously, memory 150 is provided to store data and one or more programs for interfacing with the improved sensor of the present invention. Furthermore, memory 150 may include programs for performing further digital signal processing (DSP) on pixel data or image data. Processor 140 may be a microcontroller, such as an MC251 manufactured by the assignee of the present invention. The processor 140, under the direction of a DSP program, may perform local DSP functions.

If the digital processing of the image is deferred until the data is transferred to a personal computer (PC), the image processing program may be

executed on the host processor (not shown) of the PC. The host processor may be a Pentium[®] processor with MMX[™] technology sold by the assignee of the present invention.

Figure 2 illustrates the improved pixel cell 106 configured in accordance with the teachings of one embodiment of the present invention. Each pixel cell 102 includes a first input for receiving a first reset signal (hereinafter referred to as the "PG signal"), a second input for receiving a second reset signal (hereinafter referred to as the "IG signal"), a third input for receiving a transfer signal (hereinafter referred to as the "TX signal"), a fourth input for receiving a first readout signal (hereinafter referred to as the "RS1 signal"), and a fifth input for receiving a second readout signal (hereinafter referred to as the "RS2 signal").

Each pixel cell 102 includes a first node 254 for collecting light and a second node 267 that acts as a temporary storage element. Each pixel cell 102 also includes a third node 220 for providing a first pixel value (hereinafter referred to as the "V_OUT1 signal") and a fourth node 224 for providing a second pixel value (hereinafter referred to as the "V_OUT2 signal").

As will be described in further detail with reference to Figure 4, a controller that controls the sensor employs the first reset signal and the second reset signal to reset the first node and second node, respectively. Moreover, the controller employs the transfer signal to transfer data between the first and second nodes. Two captures are performed at the same time on the same pixel, with one capture having a longer integration time than the other. The controller employs the first readout signal to readout a first pixel value from the first node and the second readout signal to readout the second pixel value from the second node. For the sake of clarity, Table I is provided that sets forth the signal names and the corresponding signal descriptions for one embodiment of the present invention.

Table I

Signal	Description
PG	First reset signal employed to reset the first node
IG	Second reset signal employed to reset the second node
TX	Transfer signal employed to transfer a pixel value from the first node to the second node
RS1	First readout signal employed to read the first node
RS2	Second readout signal employed to read the second node
V_OUT1	First pixel value corresponding to the first node
V_OUT2	Second pixel value corresponding to the second node

The pixel cell 102 is also provided with the following power voltages (VDD, V1 and V2). In the preferred embodiment, VDD is approximately equal to 3.3V, and V1 and V2 are approximately equal to zero volts.

The pixel cell 102 also includes a first readout circuit 270 and a second readout circuit 280. In response to the control signals RS1 and RS2, the first readout circuit 270 and the second readout circuit 280 selectively provide the V_OUT1 signal and the V_OUT2 signal at the third node 220 and fourth node 224, respectively.

Figure 3 is a simplified block diagram illustrating a pixel array 104 employing the pixel cells 106 and the focal plane processors 120 of the present invention. The pixel array 104 includes a plurality of pixel cells arranged in rows and columns. For each column, there is a first conductor 114 for providing the V_OUT1 signal and a second conductor 116 for providing the V_OUT2 signal. There is a focal plane processor 120 for each column. Similarly, there is an interface circuit (not shown) for each column.

Figure 4 is a flowchart illustrating how a signal processing program may employ the improved sensor to capture and process image data in accordance with one embodiment of the present invention. In step 402, the controller asserts the first reset signal (PG) to reset node 254 by device 250 and diffusion 256 to a predetermined voltage (e.g., approximately 0V). In step 404, the controller asserts the second reset signal (IG) to reset node 267 by device 284 and node 286 to the predetermined voltage. In step 406, an image is collected on node 254.

In step 408, the controller asserts the transfer signal (TX) to transfer the pixel value on node 254 to node 267 by employing device 268 at a time T1. After this transfer, node 267 contains the value corresponding to a pixel capture with an integration time period of time T1 (a first pixel value). In step 410, after an additional time period of time T2, node 254 will be at another value (a second pixel value) due to further integration of an additional time period of T2. The controller asserts the first readout signal (RS1) to read node 254 through a first readout circuit 270. The second pixel value (V_OUT1) on node 254 is provided to the third node 220. In addition, the controller asserts the second readout signal (RS2) to read node 267 (containing the first pixel value) through the second readout circuit 280. The first pixel value (V_OUT2) on node 267 is provided to the fourth node 224. Thus, V_OUT1 and V_OUT2 is output at a time period of time T1+T2.

In step 412, first integration value (V_OUT2) and second integration value (V_OUT1) are processed to arrive at a final output signal representing a pixel capture with a greater dynamic range. For example, V_OUT1 and V_OUT2 can be ratioed or have different gain curves applied to them. In this embodiment, processing step 412 determines a weighted average between V_OUT1 and V_OUT2 using pre-processing unit 116. Depending on the application, other operations such as a statistical value generation may be preferred or needed.

The operation of the pixel cell, the focal plane processor, and the interface circuit may be affected by user inputs. These user inputs may include, but are not limited to, picture size (e.g., a wide angle picture or a close-up picture), light levels, exposure time, selected compression algorithm (e.g., an amount of lossiness allowed for in the compression), and the use of flash in taking the picture.

The user inputs that are most influential in the present invention are 1) the amount of compression, and 2) the type of compression. As the amount of compression increases, the compressed signal loses picture information. Moreover, a longer time is needed to perform the compression. The processing time involved to perform the compression may affect a system designer's decision whether to integrate a signal processing circuit with the pixel cell or to employ a circuit external to the pixel cell, to perform the compression outside of each pixel cell.

These user inputs may also affect how much dynamic range compensation is used in the system. Once a user specifies these factors, a host processor or microcontroller, executing firmware or software, generates appropriate control signals and timing signals based on these factors.

Figure 5 is a block diagram of an image capture device 500 (e.g., a digital camera) in which the improved sensor 504 (hereinafter referred to as a sensor functional block (SFB)) of the present invention may be implemented. The sensor functional block (SFB) 504 may include the improved pixel cell 102, the focal plane processor 120, and interface circuit 124 described in Figure 1. The SFB 504 is coupled to a digital signal processing functional block (SPFB) 508 via a first bus 512. Data and control signals are communicated between the SFB 504 and the SPFB 508 through the first bus 512. The SPFB 508 also includes an input for user input. The user input may include an aperture setting, a shutter speed setting, and a desired resolution setting.

The information may be transferred between SPFB 508 and SFB 504 through a serial or parallel bus. The control signals for this bus are the typical read/write signals, data signals and clock signal. The sensor 504 includes a plurality of registers that store and provide control signals, timing signals and start/stop signals for the sensor 504. These functions may include integration time, and information to specify which rows and columns to read. Other signals include a start/stop signal for controlling the transfer of data from the sensor to the host processor or memory. This start/stop signal may act as an interrupt signal to suspend the operation of the sensor for short periods of time. Other signals may include outputs provided by the sensor to indicate end-of-frame, end-of-line, and the start-of-frame.

The SPFB 508 also includes an input for receiving user inputs as described previously. Depending on camera model and complexity of the camera, set exposure time, window size, and aperture. In general, these are inputs that are selected by a switch or multi-push button that the microcontroller may "read". The SPFB then turns these user inputs into a code that it writes via the 512 bus to specific register in the sensor.

Although in the preferred embodiment, the sensor functional block 504 is implemented by employing complementary metal oxide semiconductor technology (CMOS), it will be understood by those skilled in the art that the SFB 504 may be implemented using standard CCD processes. The principal

difference between a sensor functional block 504 implemented using a CCD process, as opposed to a CMOS process, is that the sensor functional block 504 implemented with a CCD process, generates an analog input, whereas the sensor functional block 504, implemented as in a CMOS process, includes analog to digital converters. Consequently, a signal functional block 504, implemented with a CMOS process, generates a digital image output.

A storage unit 516 is coupled to the SPFB 508 via a second bus 520. The storage unit 516 may be a embedded memory unit (e.g., FLASH memory) or any of the removable memory unit (e.g., Miniature Card). The removable memory unit may be employed to transfer data from image capture device to the PC for further processing, provided that the PC is equipped with the appropriate receptacles for the removable memory unit. As an example, with a PC Card adapter, image files on a Miniature Card may be transferred to any laptop or desktop PC that has a PC Card slot and the image data may then be viewed, edited, enhanced, or otherwise processed on the PC or be transmitted from the PC over a computer network to other devices connected to the network for printing, sharing, or other appropriate processing.

An interface functional block 518 is also coupled to the SPFB 508 via the second bus 520. The interface functional block 518 translates the data in a second bus format into a format acceptable to a display device (e.g., NTSC format or monitor format, or still image format) or to a personal computer (PC) via serial bus (e.g., USB protocol and/or RS-232 protocol).

Figure 6 is a block diagram illustrating in greater detail one embodiment of the SPFB 508 of Figure 5. The SPFB 508 includes a sensor timing and control functional block 636 that is coupled to the SFB 504 via the first bus 512. The sensor timing and control functional block 636 generate timing and control signals. The sensor timing and control functional block 636 may be implemented with a custom gate array or a programmable logic array (PLA) or any other suitable integrated circuits.

A direct memory access unit (DMA) 650 is coupled to the first bus 512 and the second bus 520 and buffers and transfers data between the SFB 504 to the storage unit 516 and the interface functional block 518. The DMA unit 650 is well-known in the art and will not be described herein.

The SPFB 508 also includes a digital signal processing (DSP) functional block 640. In the preferred embodiment, the DSP functional block 640 is

coupled to the first bus 504. In alternative embodiments, the DSP functional block 640 is coupled to the second bus 520 or to sensor timing and control functional block 636 and the read only memory 660. It will be understood that the general architecture described in Figures 5 and 6 may be modified to suit a particular application or optimize a specific camera system implementation.

The DSP functional block 640 is configured to perform specific signal processing operations such as noise removal, compression and other signal processing operations.

A memory or storage unit 660 such as a read only memory (ROM) is coupled to the DSP functional block 640. The unit 660 may store specific instructions such as a signal processing program 664 and a light metering program 668.

The DSP functional block 640 may be implemented by a custom application specific integrated circuit (ASIC), a custom gate array, or a microcontroller having specific DSP hardware configured around the microcontroller, or any other suitable integrated circuits. For a microcontroller-based approach, an Intel 80296 or 80X296 microcontroller may be employed.

Although Figure 6 illustrates the memory or storage unit 660 as a separate component from the DSP functional block 640, it will be known by those skilled in the art that the unit 660 and the associated programs (e.g., image compression schemes) may be embedded in the DSP functional block 640. For example, the ROM and associated programs may be embedded in a microcontroller that is used to implement the DSP functional block 640.

Figure 7 illustrates a computer system having a silicon eye in which the improved sensor of the present invention may be implemented. The computer system 700 includes a display device 702 having a silicon eye 704. The computer system 700 may also optionally include a keyboard 708, a microphone (not shown), a mouse (not shown), or any other appropriate input devices for receiving user input. The silicon eye 704 is coupled to the personal computer (PC) 720 via appropriate connecting devices such a serial cable 730, or an inferred connector (not shown). The serial cable 730 may be coupled to the PC 720 via a serial port conforming to a serial port standard (such as RS232 or UCB). The inferred connection may be implemented in accordance with methods well known in the art. As will be described in greater detail in Figure

8, the image signal is then stored and processed by the microprocessor 780, disposed on a motherboard 750.

Figure 8 is a block diagram illustrating in greater detail the computer system, shown in Figure 7. In a computer system having the silicon eye, the SPFB 816 and the interface functional block 822 are integrated with the sensor functional block 812 to comprise elements of the silicon eye 804. The silicon eye 804 also includes optics (not shown) for receiving light, an input for receiving user input, and includes an output for generating the digital image in a serial format through an appropriate connecting device such as a serial cable 830, or an inferred connector.

On the motherboard, an optional interface functional block 840 may be provided to translate the image information from one format into another and/or to further conform the image to a protocol supported by a bus 844.

The storage unit 816, illustrated in the digital image capture device, is not needed in this embodiment since memory 850 of the computer system may be employed to store the image. The memory 850 may be dynamic random access memory (DRAM), a hard drive, or any other appropriate storage device in a computer system.

A microcontroller 808, described in connection with the image capture device, is also no longer necessary in this embodiment since a processor 880 of the computer system may be employed to perform the signal processing and/or any light metering processing needed. The processor 880 may be a Pentium[®] processor with MMX[™] technology sold by the assignee of the present invention.

Moreover, the memory 850 may store the signal processing program 864 and the light metering processing program 868 that was stored in the ROM in an image capture device. The memory 850, the processor 880, and the interface functional block 840 communicate with each other through a bus 844.

The exemplary embodiments described herein are provided merely to illustrate the principles of the invention and should not be construed as limiting the scope of the invention. Rather, the principles of the invention may be applied to a wide range of systems to achieve the advantages described herein and to achieve other advantages or to satisfy other objectives as well.

CLAIMS:

1. In an image capture system having a sensor, the sensor having a first node and a second node, a method of capturing image data comprising the steps of:

- a) resetting the first node;
- b) resetting the second node;
- c) collecting an image on the first node;
- d) transferring a first pixel value from the first node to the second node after a first predetermined time period;
- e) reading a second pixel value from the first node and the first pixel value from the second node after a second predetermined time period;
- f) performing an arithmetic operation on the first pixel value and the second pixel value to generate a result; and
- g) providing the result to the image capture system.

2. The method of claim 1 wherein the step of performing an arithmetic operation on the first pixel value and the second pixel value includes the step of determining a weighted average between the first pixel value and the second pixel value.

3. The method of claim 1, wherein the step of providing the result to the image capture system includes the step of performing an analog-to-digital conversion on the result.

4. The method of claim 1, wherein the step of performing an arithmetic operation on the first pixel value and the second pixel value includes the step of performing an analog-to-digital conversion on the first pixel value and the second pixel value before the arithmetic operation is performed.

5. The method of claim 1, wherein the first node and the second node are substantially segregated electronically other than when the transfer signal is asserted.

6. In an image capture system having a sensor and a controller for controlling the sensor, the sensor including a pixel array having a plurality of pixel cells arranged in rows and columns, each pixel cell having a first node for collecting an image, a second node, a third node for providing a first pixel value and a fourth node for providing a second pixel value, a focal plane processor for processing the first pixel value and second pixel value, a method of capturing image data comprising the steps of:

- a) the controller asserting a first reset signal to reset the first node to a predetermined value;
- b) the controller asserting a second reset signal to reset the second node to the predetermined value;
- c) the pixel cell collecting an image on the first node represented by the first pixel value;
- d) the controller asserting a first transfer signal to transfer the first pixel value from the first node to the second node after a first predetermined time period;
- e) the controller asserting a first readout signal to read a second pixel value from the first node to the third node and to provide a second readout signal to read the first pixel value from the second node to the fourth node;
- f) the focal plane processor performing an arithmetic operation on the first pixel value and the second pixel value to generate a result; and
- g) the focal plane processor providing the result to the image capture system.

7. The method of claim 6 wherein the step of the focal plane processor performing an arithmetic operation includes determining a weighted average between the first pixel value and the second pixel value.

8. The method of claim 6, wherein the step of the focal plane processor providing the result to the image capture system includes the step of the focal plane processor performing an analog-to-digital conversion on the result.

9. The method of claim 6 wherein the predetermined value is approximately 0 volts.

10. The method of claim 7, wherein the step of the focal plane processor performing an arithmetic operation on the first pixel value and the second pixel value includes the step of the focal plane processor performing an analog-to-digital conversion on the first pixel value and the second pixel value before the arithmetic operation is performed

11. The method of claim 6, wherein the controller keeps the first node and the second node substantially segregated electronically other than when the first transfer signal is asserted.

12. An image capture system comprising:

- a) a sensor for capturing image data having
 - i) a pixel array having a plurality of pixel cells arranged in rows and columns, each pixel cell having a first node for collecting image data, a second node, a third node for providing a first pixel value, and a fourth node for providing a second pixel value;
 - ii) a first data conductor, coupled to the third node for communicating the first pixel value;
 - iii) a second data conductor, coupled to the fourth node for communicating the second pixel value;
 - iv) a focal plane processor coupled to the first data conductor and the second data conductor for receiving the first pixel value and the second pixel value, respectively, and responsive thereto performing an arithmetic operation on the first pixel value and the second pixel value to generate a result, the focal plane processor having an output for providing the result;
 - v) an interface circuit, coupled to the output of each focal plane processor, for interfacing the focal plane processor to a bus; and
- b) a controller, coupled to the sensor, for controlling the sensor via control signals, the control signals including a first reset signal, a second reset signal, a transfer signal, an first readout signal and an second readout signal, the controller for managing the transfer of data from the pixel cell to the focal plane processor, for controlling the focal plane processor, for managing the

transfer of data from the focal plane processor to the interface circuit, for controlling the interface circuit and for managing the transfer of data to the bus;

whereby the controller controls the sensor to generate, from the same image data, the first pixel value having a different integration time than the second pixel value.

13. The image capture system of claim 12 wherein the controller is an Intel 80296 microcontroller.

14. The image capture system of claim 12 wherein the focal plane processor includes a weighted average circuit.

15. The image capture system of claim 12 wherein each pixel cell includes a first readout circuit for providing the first pixel value and a second readout circuit for providing the second pixel value.

16. The image capture system of claim 15 wherein the interface circuit includes a correlated double sampler.

17. The image capture system of claim 16 wherein the interface circuit further includes an amplifier coupled to the correlated double sampler for providing gain to the output of the correlated double sampler.

18. The image capture system of claim 17 wherein the interface circuit further includes an analog-to-digital converter coupled to the amplifier for converting the analog output of the amplifier to a digital value suitable for transmission on the bus.