GR 95 P 4403 P

Description

Arrangement with master and slave units

The invention relates to an arrangement with at least one master unit, which is connected via a bus to slave units each having a memory, the data records of which are accessed by the master unit in a reading and/or writing manner.

An arrangement of this type is disclosed in the Siemens Catalogue ST 54.1, SIMATIC S5, Automatisierungsgeräte [Automation Devices], 1994 edition. In a mounting rack of a high-availability automation device, a plurality of master units in the form of central assemblies are connected via a parallel backplane bus to a plurality of slave units, which are designed as digital input/output assemblies, analog input/output assemblies, signal preprocessing assemblies or as communications assemblies. The master units access the slave units in a reading or writing manner, and various types of data, for example process data, parameterization data or diagnostic data, are exchanged between the master and slave units. For this purpose, the slave units usually have a memory, in which the data are stored in areas which are provided therefore and are accessed by the master units using corresponding addresses. In order to enable fault-free access to these data, the master units must know both the size of the memory and its division into the different areas and the type and arrangement of the various data types within these areas. If, for example, a master unit attempts to access diagnostic data of a slave unit which is not equipped with diagnostic functionality and is therefore not provided with any diagnostic data, then no faults, for example in the form of prolonged bus occupancy, are permitted to occur, particularly in automation devices. In order to avoid such faults, it is possible to provide all of the slave units which are connected to the bus with memories

of the same size and to configure the division of the areas and the type and arrangement of the data uniformly. However, this means adapting the respective memory of the slave units both to the largest memory and to the largest memory area of the arrangement. As a result, a number of slave memories are oversized, and the size of the memory areas cannot be varied.

German Patent Application P 44 40 789.0 proposes an arrangement with at least one master unit, which is connected via a bus to slave units each having a memory, the master unit executing read and/or write accesses to the said memory. The slave units each have a protocol area, by means of which the master unit indicates to the slave unit an imminent memory access, the respective slave unit granting or denying the master unit access authorization by means of this protocol area, in which case, in the event of access authorization, the slave unit allocates to the master unit an address range of the memory, the position of which the master unit reads out from the protocol area. The address range of the slave memory is thus dependent on the bus address range.

The present invention is based on the object of specifying an arrangement of the type mentioned in the introduction in which the master unit initiates data access uniformly to each of the slave units according to a predetermined communications protocol. Furthermore, the intention is to provide a slave unit which is suitable for communication with a master unit according to this protocol.

This object is achieved, with regard to the arrangement, by means of the measures specified in the characterizing part of Claim 1 and, with regard to the slave unit, by means of the measures specified in Claim 10.

All of the slave units which are connected to the bus are provided with the protocol area which is accessed by the master unit uniformly in a reading or writing manner. The intended communication with a slave unit is indicated by the master unit to the slave unit in a job cell of the protocol area, and is acknowledged by the slave unit by means of an entry in a response cell of this protocol area. The master unit always addresses the job and response cells of the slave units participating in the communication under the same addresses. If the slave unit grants access authorization, the slave unit enters into the response cell the transfer address under which the master unit accesses a data record or a plurality of data records. The end of a data transmission is indicated by the master unit to the slave unit by means of a corresponding entry in the job cell, which the slave unit in turn acknowledges with an entry in the response cell.

All of the data record accesses made by the master unit are carried out under the same transfer address, the bit width of which preferably corresponds to that of the bus. The addresses allocated by the slave unit to the data records for the purpose of storage in the memory differ from the transfer address. The address range of the slave memory is thus independent of the bus address range, and the size of the memory can be adapted to the requirements of the slave unit.

The slave unit itself manages its memory; the master unit knows neither the memory size nor the division of the memory into different areas, as a result of which a "catalog knowledge" of the master unit regarding the memories of the slave units is unnecessary and delay times are shortened. The size and division of this memory depend exclusively on the functionality of the different slave units. As a result, memory modules are saved particularly in the case of slave units which, for example, are provided only with diagnostic data or which cannot process any data records at all and therefore do not have a memory for process data, parameterization data and

diagnostic data.

The data records to be written in or read out are each provided with a data record number, and, in the event of a write access, the master unit enters the length of a data record to be written in into the job cell and, in the event of a read access, the slave unit enters the length of a data record to be read out into the response cell. By virtue of these length details, various data records, for example 8-, 16- or 32-byte data records, are supported, and slave units can be expanded by new functions which require an enlargement of the memory and of the data records without disturbances to the arrangement.

In order that these slave units which have no memory at all for such data records can participate in the communications protocol, the master unit is always denied access to data records by means of a permanently set identifier in the response cell. The master unit usually accesses such slave units, for example slave units in the form of digital input/output units, with an insertion location address and an identifier for the input or output to be addressed.

The arrangement can be expanded by further slave units having different functions, provided that the slave units provide this necessary protocol area by means of which the master unit can initiate communication with the slave units.

The arrangement may comprise a plurality of master units which are each provided with an identifier. A master unit executing a write or read access enters its identifier into the job cell, each master unit accessing a slave unit under a transfer address assigned to it.

Constituents of the communications protocol are a start telegram and an end telegram, of which the start telegram includes the entry of the identifier for the beginning of a data record access and the end telegram includes the entry of the identifier for the end of a data record access. A start telegram interrupts a current data record access. In this case,

the data record number and the memory address range of the data, still to be transmitted, of the data record are stored in a protocol memory of the slave unit. The protocol memory of the slave units is subdivided into areas, one area being assigned to each master unit. As a result, the correct assignment between job and response is ensured both for the respective master unit and for the slave unit, and the slave units can communicate with the individual master units in a targeted manner.

Further refinements of the invention emerge from the further subclaims.

The invention is employed particularly in automation devices.

The invention and its refinements and advantages are explained in more detail with reference to the drawing, in which an exemplary embodiment of the invention is illustrated and in which:

Figure 1 shows a protocol area of a slave unit,

Figures 2 to 4 show functional illustrations of a slave unit memory management and,

Figure 5 shows the block diagram of an evaluation circuit of a slave unit.

Figure 1 illustrates a protocol area of a slave assembly which comprises a job cell 1 and a response cell 2, of which the job cell 1 comprises three registers 3, 4, 5 and the response cell 2 comprises two registers 6, 7. The registers 3 ... 7 can be addressed using addresses ad1 ... ad5, a master unit accessing the registers 3, 4, 5 in a writing manner and the registers 6, 7 in a reading manner, and the slave unit accessing the registers 6, 7 in a writing manner and the registers 3, 4, 5 in a reading manner. In order to initiate a memory access, the master unit first of all enters a plurality of identifiers

into the register 3, to be precise an identifier for the imminent write or read access into the cell 0 of the register 3, an identifier for the beginning of the access into the cells 1 and 2 and an identifier for the accessing master unit into the cells 6 and 7. The cells 3 ... 5 are not written to, rather are reserved for possible functional expansions. The master unit stores in the register 4 the number of a data record which is to be entered into the memory of the slave unit or is to be read out therefrom. In the event of a write access, the master unit stores in the register 5 an identifier for the length of the data record to be written in. In the event of a read access, on the other hand, the slave unit stores in the register 6 the identifier for the length of the data record to be read out. This means that, in the event of a write access, the master unit writes to the registers 3, 4, 5 of the job cell which the slave unit reads out, and that the slave unit writes only to the register 7 which the master unit reads out. In the event of a read access to be initiated, on the other hand, the master unit writes only to the registers 3, 4 and the slave unit, in addition to the register 7, writes to the register 6 of the response cell. The slave unit indicates to the master unit whether the master unit is authorized to execute a read access to the data record indicated by the data records number or to enter this data record into the memory of the slave unit by means of a corresponding entry in the cells 0 and 1 of the register 7. In this case, the slave unit can indicate that this master unit temporarily cannot access the data record specified, because the slave unit is currently processing the data record, that the master unit cannot access the data record at all, for example because the slave unit has no knowledge whatsoever of the requested data record, or that the master unit can access the data record requested, in this case the slave unit indicating to the master unit a transfer address, under which the master unit accesses data records, in the cells 2 ... 6 of the register 7. The cell 7 of the register 7 is not occupied

and

can likewise be taken into account for possible functional expansions.

After the entries in the registers 3 ... 7, the master unit, in the event of access authorization existing, accesses the data stored in the memory of the slave unit under the transfer address specified, that is to say the data transmission between the slave unit and the master unit is carried out under this address. The end of the access is indicated by the master unit to the slave unit by means of a renewed entry of a corresponding identifier into the cells 1 and 2 of the register 3. The slave unit acknowledges the end of the access by writing the identifier provided therefore to the cells 0 and 1 of the register 7.

In a practical exemplary embodiment of the invention, the following identifiers are provided for the registers 3 ... 7:

Cells 6 and 7 of the register 3:

00 = master unit 1
01 = master unit 2
10 = master unit 3
11 = master unit 4

Cells 1 and 2 of the register 3:

00 = reserved
01 = beginning of the access
10 = end of the access
11 = termination/reset

Cell 0 of the register 3:

0 = write
1 = read

Number of the data record in register 4:

0 ... 255

Length (in bytes) of the data record in registers 5 and 6:

0 ... 255

Cells 0 and 1 in register 7:

00 = reserved
01 = acknowledgement negative (temporarily)
10 = acknowledgement positive
11 = acknowledgement negative (generally, i.e. slave unit does not know the number of the data record)

Cells 2 ... 6 in register 7:

12 = transfer address 176
13 = transfer address 180
14 = transfer address 184
15 = transfer address 188
16 = transfer address 192
17 = transfer address 196
18 = transfer address 200
19 = transfer address 204
20 = transfer address 208
21 = transfer address 212
.
.
.

Cells 3 ... 5 of the register 3 and cell 7 of the register 7 are reserved.

Figure 2 illustrates a memory 10 of a slave unit into which a user must enter parameter data

in order to parameterize the slave unit. Identical parts appearing in Figures 1 and 2 are provided with identical reference signals, the protocol area being a component part of a protocol memory 8 in the present example. Parameterization requires the user to store the parameters in a data record with the data record number 30 in accordance with a parameterization convention provided for this unit. The master unit activates a write signal WR for writing to the protocol memory 8 and writes to the register 3 of the job cell the identifier 0 (cell 0, Figure 1) for an intended write access and the identifier 01 (not illustrated) for the beginning of the write access (cells 1 and 2, Figure 1), to the register 4 the number 30 of the parameterization data record and to the register 5 the length lae30 of this data record. The slave unit first of all reads out the contents of the registers 3, 4 and uses the table 9 stored in the slave unit to identify that authorization (identifier 10) exists for a write access for writing in the parameterization data record number 30. The slave unit subsequently transfers the length lae30 of the data record to the table, assigns to this data record an identifier 12 for the transfer addresses 176, 177, 178 and 179 and writes this identifier 12 to the register 7 (cell 2 ... 6, Figure 1). The master unit now activates a read signal RD for reading out the contents of the register 7 and, in a next step, writes the parameterization data record having the length lae30 to the protocol memory 8 under the transfer addresses 176 ... 179. The slave unit allocates an address adr30 to this data record and stores the data record in its memory 10 under this address. Of course, it may be necessary for the master unit to write to the protocol area of the transfer addresses 176 .. 179 a number of times, and for the slave unit to read out this area a number of times. This is the case, for example, when the data record length is greater than 4 bytes and the width of the protocol memory is only 8 bits, which means that the master unit can only read out 4 bytes during a data record access.

After the master unit has completely transmitted the data record with the data record number 30 to the slave unit by way of the transfer addresses 176 ... 179, the master unit indicates the end of the write access (not illustrated) to the slave unit. For this purpose, the master unit again activates the write signal and enters the identifier 10 for the end of the access into the register 3. The slave unit reads out the register 3 and acknowledges by entering the identifier 11 (positive acknowledgement) into the register 7 of the response cell. The write access is thus ended.

Figure 3 illustrates a read access to the memory 10 of the slave unit. It is assumed here that a data record with the number 40 is to be read out. The master unit first of all activates the write signal WR and enters into the register 3 the identifier 1 one for an intended read access, the identifier 01 (not illustrated) for the beginning of the access, and into the register 4 the number 40 of the data record to be read out. The slave unit reads out the registers 3 and 4 and, since authorization exists (identifier 10 in table 9) for a read access to the data record number 40, the slave unit enters the length of the data record lae40 and the identifier 12 for the transfer addresses 176, 177, 178 and 179 from the table 9 and into the registers 6 and 7 of the response cell 2. After activation of the read signal RD, the master unit reads out the contents of the registers 6 and 7 and accesses those contents (data record number 40) of the protocol memory under the transfer addresses 176 ... 179 which the slave unit has read out from the memory 10 under the address adr40 and has entered into the protocol memory under these transfer addresses. The read access, too, may require the slave unit to write a number of times to the protocol area with the transfer addresses 176 .. 179, depending on the length of the data record to be read out and on the width of the protocol memory, and the master unit to read out this area a number of times, in order to read out the data record completely. The end of the read access is

indicated by the master unit once again in the register 3 to the slave unit, which acknowledges the indication in the register 7.

In Figure 4, the protocol memory 8 is provided with four stack areas SB1 ... SB4, which are respectively assigned to one of four master units with the identifiers 00, 01, 10 and 11 (Figure 1). The generality is not restricted by the fact that the protocol area 1, 2 and the protocol memory 8 as well as the control table 9 and the slave memory 10 are illustrated separately. It goes without saying that a division of the areas in accordance with Figures 2 and 3 or another suitable division is also conceivable.

It is initially assumed that - as already described - the master unit 1 (identifier 00) initiates the access to a data record with a first start telegram, which includes the entry of the identifier for the beginning of an access and the identifier 00 for the accessing master unit. A protocol controller 11 of the slave unit reads the start telegram from the job cell 1, checks the access authorization and, in the event of granted access authorization, writes to the response cell 2 the identifier 12 for transfer addresses 176 ... 179, which is assigned to this master unit 1. The master unit 1 accesses those registers of the slave unit which can be addressed under these transfer addresses and to or from which the slave unit writes or reads the requested data. It may now happen that, on account of stipulations of a control program to be processed by the master unit 1, this data record access must be interrupted and the master unit 1 must access a different data record. For this purpose, the master unit 1 writes a second start telegram to the job cell 1, the effect of which is that the protocol controller 11 first of all enters into the stack store SB1 the current data record number nr_akt of the data record whose transmission has been interrupted, the data record length lae_akt of this data record which is still to be transmitted and the current memory address adr_akt under which the data which have not yet been transmitted

are stored in the slave memory 10.

After this data protection, the slave unit processes the data transfer initiated by the second start telegram. If this data transfer is concluded, which the master unit 1 indicates to the slave unit by means of an end telegram, the data transmission of the interrupted data transfer is resumed. For this purpose, it is first of all necessary for the protocol controller 11 first of all to read in the information items (the data record number nr_akt, data record length lae_akt, memory address adr_akt) which are stored in the stack area SB1, in order to continue the data transmission. The end of the transmission is indicated by the master unit 1 to the slave unit once again by an end telegram assigned to this data record.

The processing of protocols of a plurality of master units by the slave unit is considered in the following text. It is assumed here that the master unit 2 enters a start telegram into the job cell 1 for a write access to a data record which the master unit 1 is currently accessing in a writing manner (nested write accesses). In this case, the slave unit acknowledges the access of this master unit 2 temporarily negatively (identifier 01, Figure 1) in the response cell 2. Nested read accesses, that is to say read accesses by a plurality of master units to the same data record, are possible, in which case the "nesting depth" should not be selected to be excessively high for reasons of performance. Each master unit is assigned a dedicated transfer address under which the respective master unit accesses data records. In order to enable simultaneous, nested write and read accesses to a data record, the slave memory 10 is subdivided into a writing area and a reading area. A data record which has been modified by a write access is stored by the slave unit after this modification in the reading area, in each case the same data record number being assigned to these data records.

In order to achieve a deterministic behavior, all of the slave units must acknowledge accesses by the master unit within a specific time. If a plurality of master units wish to access a data record, it is necessary for the slave unit to positively acknowledge the intended access to the master unit which is effecting access first, and on the other hand to temporarily negatively acknowledge the access attempt to all the other master units.

Figure 5 shows the block diagram of a simple evaluation circuit of a slave unit which is suitable for evaluating three different data records which are provided with data record numbers 51, 52, 53. A write access is considered in the following text. The corresponding identifiers which are to be evaluated are fed to the job cell 1 via a bus BU during the active write signal WR. In the present example, however, an identifier MK of the accessing master unit and the data record length lae are not evaluated. Data records are connected to comparators V1, V2, V3, which check whether the master unit is authorized to access the data records 51, 52, 53. The identifiers Ke for the beginning of the job, the end of the job or termination of the job are checked by means of discrete logic. An encoder EN assigns a transfer address Adr to the data records and, if an access to one of the data records 51, 52, 53 and the identifier Ke is permissible, a positive acknowledgement is stored in the response register 2. The response cell 2 is read out by the master unit during the active read signal RD, and, by way of the transfer address Adr which has been read out, the data records 51, 52, 53 are transmitted between the master unit and the slave unit. Identification and mutual interlocking of multiple jobs is not possible using the simple evaluation circuit illustrated.

Patent Claims

1. Arrangement with at least one master unit, which is connected via a bus to slave units each having a memory, the data records of which are accessed by the master unit in a reading or writing manner,
characterized

- in that the slave units each have a protocol area (1, 2) which can be written to for a communications protocol and by means of which the master unit indicates to the respective slave unit an imminent memory access and this slave unit grants or denies the master unit access authorization, and
- in that, in the event of access authorization, the respective slave unit allocates to the master unit at least one transfer address, which the master unit reads out from the protocol area and under which the master unit accesses the data records.

2. Arrangement according to Claim 1, characterized

- in that the slave units allocate to the data records addresses for storage in their memory.

3. Arrangement according to Claim 1 or 2, characterized

- in that the same transfer address is provided for each data access by the master unit.

4. Arrangement according to one of Claims 1 to 3, characterized

- in that the protocol area comprises a job cell (1) and a response cell (2) of which the master unit writes to the job cell (1) a write or read identifier, an identifier for the beginning and/or the end of an access, and, in the event of a write access, a length identifier (lae30) of a data record to be written in,

* C L M S *

and the slave unit writes to the response cell (2) an identifier for the access authorization, the transfer address, and, in the event of a read access, a length identifier (lae40) of a data record to be read out.

5. Arrangement according to one of Claims 1 to 4, characterized

- in that the data records are provided with data record numbers (30, 40), which the master unit enters into the job cell (1).

6. Arrangement according to Claim 1 to 5, characterized

- in that the communications protocol comprises a start telegram and an end telegram, the start telegram including the entry of the identifier for the beginning of a data record access, and the end telegram including the entry of the identifier for the end of a data record access.

7. Arrangement according to Claim 6, characterized

- in that a start telegram interrupts a current data record access, and
- in that the slave units are provided with a protocol memory, in which, for the interrupted data record access, the data record number and the memory address range of the data, still to be transmitted, of the data record are stored.

8. Arrangement according to one of Claims 1 to 7, characterized,

- in that the arrangement has at least one further master unit,
- in that each master unit is provided with an identifier,
- in that the master unit executing a data record access enters its identifier into the protocol area, and

* C L M S *

- in that different transfer addresses are provided for the master units.

9. Arrangement according to one of Claims 1 to 8, characterized by

- a further slave unit provided with a protocol area, the protocol area comprising a response cell which is provided with a fixed identifier which the master unit reads out and the effect of which is that the slave unit denies the master unit a read and/or write access.

10. Slave unit, suitable for an arrangement according to one of Claims 1 to 9.

11. Automation device having an arrangement according to one of Claims 1 to 9.

