CLAIMS

1. A method for performing low-density parity-check (LDPC) decoding, the method comprising: receiving soft bits associated to an LDPC codeword; and performing LDPC decoding of the soft bits using a parity check matrix, wherein: the parity check matrix comprises: a core portion of a first N rows; and hybrid automatic repeat request (HARQ) rows after the first N rows; each row of the parity check matrix corresponds to a lifted parity check of a lifted LDPC code; at least two columns of the parity check matrix correspond to punctured variable nodes of the lifted LDPC code; and the parity check matrix has row orthogonality between each pair of consecutive rows that are below a lowest row to which the at least two punctured variable nodes are both connected, wherein for each row below the lowest row to which the at least two punctured variable nodes are both connected, no column has a non-empty entry in two consecutive rows.

2. The method of claim 1, wherein in each pair of consecutive rows the two punctured variable nodes alternate connections to subsequent rows.

3. The method of claim 1, wherein at least 1/2 of all pairs of consecutive rows of the parity check matrix have row orthogonality.

4. The method of claim 3, wherein the at least 1/2 of all pairs of consecutive rows comprises the last 1/2 of all rows of the parity check matrix, and wherein the last 1/2 of all rows of the parity check matrix correspond to rows associated with hybrid automatic repeat request (HARQ) information of the LDPC codeword.

5. The method of claim 1, wherein in each pair of consecutive rows below the lowest row to which the at least two punctured variable nodes are both connected, the two punctured variable nodes alternate connections to subsequent rows.

6. An apparatus for wireless communications, comprising: a processor configured to: cause the apparatus to receive soft bits associated to a low-density parity-check (LDPC) codeword; and perform LDPC decoding of the soft bits using a parity check matrix, wherein: the parity check matrix comprises: a core portion of a first N rows; and hybrid automatic repeat request (HARQ) rows after the first N rows; each row of the parity check matrix corresponds to a lifted parity check of a lifted LDPC code; at least two columns of the parity check matrix correspond to punctured variable nodes of the lifted LDPC code; and the parity check matrix has row orthogonality between each pair of consecutive rows that are below a lowest row to which the at least two punctured variable nodes are both connected, wherein for each row below the lowest row to which the at least two punctured variable nodes are both connected, no column has a non-empty entry in two consecutive rows; and a memory coupled with the processor.

7. The apparatus of claim 6, wherein in each pair of consecutive rows the two punctured variable nodes alternate connections to subsequent rows.

8. The apparatus of claim 6, wherein at least 1/2 of all pairs of consecutive rows of the parity check matrix have row orthogonality.

9. The apparatus of claim 8, wherein the at least 1/2 of all pairs of consecutive rows comprises the last 1/2 of all rows of the parity check matrix, and wherein the last 1/2 of all rows of the parity check matrix correspond to rows associated with hybrid automatic repeat request (HARQ) information of the LDPC codeword.

10. The apparatus of claim 6, wherein in each pair of consecutive rows below the lowest row to which the at least two punctured variable nodes are both connected, the two punctured variable nodes alternate connections to subsequent rows.

11. A method for performing low-density parity-check (LDPC) encoding, the method comprising: obtaining information bits of a codeword; and performing encoding of the information bits to compute parity bits of an LDPC codeword according to a parity check matrix, wherein: the parity check matrix comprises: a core portion of a first N rows; and hybrid automatic repeat request (HARQ) rows after the first N rows; each row of the parity check matrix corresponds to a lifted parity check of a lifted LDPC code, at least two columns of the parity check matrix correspond to punctured variable nodes of the lifted LDPC code, and the parity check matrix has row orthogonality between each pair of consecutive rows that are below a lowest row to which the at least two punctured variable nodes are both connected, wherein for each row below the lowest row to which the at least two punctured variable nodes are both connected, no column has a non-empty entry in two consecutive rows.

12. The method of claim 11, wherein in each pair of consecutive rows the two punctured variable nodes alternate connections to subsequent rows.

13. The method of claim 11, wherein at least 1/2 of all pairs of consecutive rows of the parity check matrix have row orthogonality.

14. The method of claim 13, wherein the at least 1/2 of all pairs of consecutive rows comprises the last 1/2 of all rows of the parity check matrix, and wherein the last 1/2 of all rows of the parity check matrix correspond to rows associated with hybrid automatic repeat request (HARQ) information of the LDPC codeword.

15. The method of claim 11, wherein in each pair of consecutive rows below the lowest row to which the at least two punctured variable nodes are both connected, the two punctured variable nodes alternate connections to subsequent rows.

16. An apparatus for wireless communications, comprising: a processor configured to: obtain information bits of a codeword; and perform encoding of the information bits to compute parity bits of an LDPC codeword according to a parity check matrix, wherein: the parity check matrix comprises: a core portion of a first N rows; and hybrid automatic repeat request (HARQ) rows

after the first N rows; each row of the parity check matrix corresponds to a lifted parity check of a lifted LDPC code, at least two columns of the parity check matrix correspond to punctured variable nodes of the lifted LDPC code, and the parity check matrix has row orthogonality between each pair of consecutive rows that are below a lowest row to which the at least two punctured variable nodes are both connected, wherein for each row below the lowest row to which the at least two punctured variable nodes are both connected, no column has a non-empty entry in two consecutive rows; and a memory coupled with the processor.

17. The apparatus of claim 16, wherein in each pair of consecutive rows the two punctured variable nodes alternate connections to subsequent rows.

18. The apparatus of claim 16, wherein at least 1/2 of all pairs of consecutive rows of the parity check matrix have row orthogonality.

19. The apparatus of claim 18, wherein the at least 1/2 of all pairs of consecutive rows comprises the last 1/2 of all rows of the parity check matrix, and wherein the last 1/2 of all rows of the parity check matrix correspond to rows associated with hybrid automatic repeat request (HARQ) information of the LDPC codeword.

20. The apparatus of claim 16, wherein in each pair of consecutive rows below the lowest row to which the at least two punctured variable nodes are both connected, the two punctured variable nodes alternate connections to subsequent rows.