METHODS OF FORMING MASK PATTERNS ON SEMICONDUCTOR WAFERS THAT COMPENSATE FOR NONUNIFORM CENTER-TO-EDGE ETCH RATES DURING PHOTOLITHOGRAPHIC PROCESSING

Abstract of the Disclosure

Methods of forming integrated circuit devices include steps to selectively widen portions of a mask pattern extending adjacent an outer edge of a semiconductor wafer. These steps to selectively widen portions of the mask pattern are performed so that more uniform center-to-edge critical dimensions (CD) can be achieved when the mask pattern is used to support photolithographically patterning of underlying layers (e.g., insulating layers, antireflective coatings, etc.).

Fig. 1