CLAIMS

1. A method of translating addresses in a computing environment, said method comprising:

obtaining an address from an adapter to be translated, the address comprising a plurality of bits, the plurality of bits comprising a first portion of bits and a second portion of bits;

receiving an address range value that indicates a range of permitted addresses;

validating the address using at least the first portion of bits and the received address range; and

converting the address to a memory address usable in accessing memory of the computing environment, the converting ignoring the first portion of bits and using the second portion of bits to obtain address information from one or more levels of address translation tables to perform the converting.

2. The method of claim 1, wherein the first portion of bits comprises high order bits of the address and the second portion of bits comprises low order bits of the address, the low order bits determined based on a size of an assigned address space that includes the memory address.

3. The method of claim 1, wherein a number of levels of address translation tables is based on at least one of a size of an assigned address space that includes the memory address, a size of one or more address translation tables to be used in the converting, and a size of the unit of memory accessed by the memory address.

4. The method of claim 1, wherein the converting comprises selecting an address translation table to be used to convert the address, the selecting using a pointer in a device table entry used in the converting.

5. The method of claim 4, wherein the method further comprises locating the device table entry, the locating using at least one of a requestor identifier of the adapter issuing a request that includes the address to be translated or a portion of the address.

6. The method of claim 4, wherein the method further comprises determining a format of the selected address translation table, the determining using a format field of the device table entry.

7. The method of claim 4, wherein the address range is defined by at least one of a base field and a limit field of the device table entry to validate the address.

8. The method of claim 7, wherein the validating the address comprises:

permitting execution responsive to determining that the first portion of bits are within a range of corresponding bits of address range, wherein the corresponding bits of the address range are not all 0's; and

no permitting execution responsive to determining that the first portion of bits are not within a range of corresponding bits of the address range, wherein the corresponding bits of the address range are not all 0's.

9. The method of claim 1, wherein the adapter comprises a function, the function comprising a Peripheral Component Interconnect function.

10. A computer system for translating addresses in a computing environment, the computer system comprising:

a memory;

a processor in communications with the memory;

an address obtainer for obtaining an address from an adapter to be translated, the address comprising a plurality of bits, the plurality of bits comprising a first portion of bits and a second portion of bits;

a receiver for receiving an address range value that indicates a range of permitted addresses;

a validator for validating the address using at least the first portion of bits and the received address range; and

a converter for converting the address to a memory address usable in accessing memory of the computing environment, the converting ignoring the first portion of bits and

using the second portion of bits to obtain address information from one or more levels of address translation tables to perform the converting.

11. A computer program comprising computer program code stored on a computer readable medium to, when loaded into a computer system and executed thereon, cause said computer system to perform all the steps of a method according to any of claims 1 to 9.

12. A computer system for translating addresses in a computing environment, the computer system comprising:

a memory; and

a processor in communications with the memory, wherein the computer system is configured to perform a method, said method comprising:

obtaining an address from an adapter to be translated, the address comprising a plurality of bits, the plurality of bits comprising a first portion of bits and a second portion of bits;

receiving an address range value that indicates a range of permitted addresses;

validating the address using at least the first portion of bits and the received address range; and

converting the address to a memory address usable in accessing memory of the computing environment, the converting ignoring the first portion of bits and using the second portion of bits to obtain address information from one or more levels of address translation tables to perform the converting.

13. The computer system of claim 12, wherein the first portion of bits comprises high order bits of the address and the second portion of bits comprises low order bits of the address, the low order bits determined based on a size of an assigned address space that includes the memory address.

14. The computer system of claim 12, wherein a number of levels of address translation tables is based on at least one of a size of an assigned address space that includes the memory address, a size of one or more address translation tables to be used in the converting, and a size of the unit of memory accessed by the memory address.

15. The computer system of claim 12, wherein the converting comprises selecting an address translation table to be used to convert the address, the selecting using a pointer in a device table entry used in the converting.

16. The computer system of claim 15, wherein the method further comprises locating the device table entry, the locating using at least one of a requestor identifier of the adapter issuing a request that includes the address to be translated or a portion of the address.

17. The computer system of claim 15, wherein the method further comprises determining a format of the selected address translation table, the determining using a format field of the device table entry.

18. The computer system of claim 15, wherein the address range is defined by at least one of a base field and a limit field of the device table entry to validate the address.

19. The computer system of claim 18, wherein the validating the address comprises:

permitting execution responsive to determining that the first portion of bits are within a range of corresponding bits of address range, wherein the corresponding bits of the address range are not all 0's; and

no permitting execution responsive to determining that the first portion of bits are not within a range of corresponding bits of the address range, wherein the corresponding bits of the address range are not all 0's.

20. The computer system of claim 12, wherein the adapter comprises a function, the function comprising a Peripheral Component Interconnect function.

21. A computer program product for translating addresses in a computing environment, the computer program product comprising:

a computer readable storage medium readable by a processing circuit and storing instructions for execution by the processing circuit for performing a method according to any of claims 1 to 9.

CLAIMS

1. A method of translating addresses in a computing environment, said method comprising:

obtaining an address from an adapter to be translated to a memory address directly usable in accessing system memory of the computing environment, the address comprising a plurality of bits, the plurality of bits comprising a first portion of bits and a second portion of bits;

receiving an address range value that indicates a range of permitted addresses, wherein the range is defined by a base address and a limit located in a device table entry associated with the adapter, the device table entry located by a requestor identifier located in a request issued by the adapter;

validating the address obtained from the adapter using at least the first portion of bits and the received address range; and

converting the address obtained from the adapter to the memory address directly usable in accessing system memory of the computing environment, the converting ignoring the first portion of bits and using the second portion of bits to obtain address information from one or more levels of address translation tables to perform the converting.

2. The method of claim 1, wherein the first portion of bits comprises high order bits of the address and the second portion of bits comprises low order bits of the address, the low order bits determined based on a size of an assigned address space that includes the memory address.

3. The method of claim 1, wherein a number of levels of address translation tables is based on at least one of a size of an assigned address space that includes the memory address, a size of one or more address translation tables to be used in the converting, and a size of the unit of memory accessed by the memory address.

4. The method of claim 1, wherein the converting comprises selecting an address translation table to be used to convert the address, the selecting using a pointer in a device table entry used in the converting.

5. The method of claim 4, wherein the method further comprises locating the device table entry, the locating using at least one of a requestor identifier of the adapter issuing a request that includes the address to be translated or a portion of the address.

6. The method of claim 4, wherein the method further comprises determining a format of the selected address translation table, the determining using a format field of the device table entry.

7. The method of claim 1, wherein the validating the address comprises:

permitting execution responsive to determining that the first portion of bits are within a range of corresponding bits of address range, wherein the corresponding bits of the address range are not all 0's; and

no permitting execution responsive to determining that the first portion of bits are not within a range of corresponding bits of the address range, wherein the corresponding bits of the address range are not all 0's.

8. The method of claim 1, wherein the adapter comprises a function, the function comprising a Peripheral Component Interconnect function.

9. A computer system for translating addresses in a computing environment, the computer system comprising:

a memory;

a processor in communications with the memory;

an address obtainer for obtaining an address from an adapter to be translated to a memory address directly usable in accessing system memory of the computing environment, the address comprising a plurality of bits, the plurality of bits comprising a first portion of bits and a second portion of bits;

a receiver for receiving an address range value that indicates a range of permitted addresses, wherein the range is defined by a base address and a limit located in a device table entry associated with the adapter, the device table entry located by a requestor identifier located in a request issued by the adapter;

a validator for validating the address obtained from the adapter using at least the first portion of bits and the received address range; and

a converter for converting the address obtained from the adapter to the memory address directly usable in accessing system memory of the computing environment, the converting ignoring the first portion of bits and using the second portion of bits to obtain address information from one or more levels of address translation tables to perform the converting.

10. A computer program product for translating addresses in a computing environment, the computer program product comprising:

a computer readable storage medium readable by a processing circuit and storing instructions for execution by the processing circuit for performing a method according to any of claims 1 to 9.

11. A system comprising means adapted for carrying out all the steps of the method according to any one of the preceding method claims.