A METHOD OF MAKING DIRECT CONTACT ON GATE BY USING DIELECTRIC STOP LAYER

ABSTRACT

A CMOS RF device and a method to fabricate said device with low gate contact resistance are described. Conventional MOS transistor is first formed with isolation regions, poly-silicon gate structure, sidewall spacers around poly gate, and implanted source/drain with lightly and heavily doped regions. A silicon dioxide layer such as TEOS is deposited, planarized with chemical mechanical polishing (CMP) to expose the gate and treated with dilute HF etchant to recess the silicon dioxide layer below the surface of the gate. Silicon nitride is then deposited and planarized with CMP and then etched except around the gates, using a oversize poly-silicon gate mask. Inter-level dielectric mask is then deposited, contact holes etched, and contact metal is deposited to form the transistor. During contact hole etch over poly-silicon gate, silicon nitride around the poly gate acts as an etch stop. Resulting structure with direct gate contact achieves significantly reduced gate resistance and thereby improved noise performance at high frequency operation, increased unit power gain frequency (f_{max}), and reduced gate delay.

Figure 6