

WHAT IS CLAIMED IS:

1. A device, comprising:

a lower layer;

an upper layer on the lower layer that defines a trench extending from a top surface of the upper layer towards the lower layer; and

a gap-fill layer filling the trench, the gap-fill layer having a multi-layered structure, the gap-fill layer including

a first dielectric layer that fills a first portion of the trench, the first dielectric layer having a top surface that is proximate to the top surface of the upper layer;

a second dielectric layer that fills a second portion of the trench, the second dielectric layer having a top surface that is proximate to the top surface of the upper layer, the top surface of the second dielectric layer is more recessed toward the lower layer than the top surface of the first dielectric layer; and

a third dielectric layer that fills a remaining portion of the trench and covers the top surface of the second dielectric layer,

wherein the first dielectric layer has a U shape,

the first dielectric layer includes two top ends on an inner sidewall surface of the trench, the two top ends of the first dielectric layer adjacent to the top surface of the upper layer,

the third dielectric layer further covers the two top ends of the first dielectric layer, and

the top surface of the first dielectric layer is located at a lower level than the top surface of the upper layer.

~~2. The device of claim 1, wherein~~

~~the first dielectric layer has a U shape, and,~~

~~the first dielectric layer includes two top ends on an inner sidewall surface of the trench, the two top ends of the first dielectric layer adjacent to the top surface of the upper layer.~~

~~3. — The device of claim 2, wherein each top end of the two top ends of the first dielectric layer is exposed at the top surface of the upper layer.~~

42. The device of claim ~~12 or claim 3~~, wherein a top surface of each top end of the two top ends of the first dielectric layer is at a level that is ~~equal to or~~ less than a level of the top surface of the upper layer over a top surface of the lower layer.

~~5. — The device of claim 2, wherein the third dielectric layer further covers the two top ends of the first dielectric layer.~~

63. The device of any one of claims 1 ~~or claim 2 to 5~~, wherein an interface between the second and third dielectric layers has a concave shape toward the lower layer.

74. The device of any one of claims 1 to 63, wherein the first dielectric layer has a density greater than a density of the second dielectric layer.

85. The device of any one of claims 1 to 74, wherein the second and third dielectric layers have a same material composition.

96. The device of any one of claims 1 to 85, wherein
the upper layer includes a plurality of stacked layers, and
the plurality of stacked layers includes a dielectric layer, a conductive layer, or a combination thereof.

407. The device of claim 1, wherein

the first dielectric layer has a ~~a~~the U shape that defines an open enclosure that is open towards the top surface of the upper layer,

the second dielectric layer fills a portion of the open enclosure of the first dielectric layer, and

the third dielectric layer fills a remaining portion of the open enclosure of the first dielectric layer.

418. A semiconductor device, comprising:

a peripheral region including a peripheral circuit, the peripheral circuit including

a plurality of transistors on a substrate, and

a plurality of electrical lines electrically connected to the plurality of transistors;

a cell region on the peripheral region, the cell region including

a semiconductor layer on the peripheral region,

an electrode stack on the semiconductor layer and overlapping the peripheral circuit in a direction that is normal to a top surface of the semiconductor layer, the electrode stack having a stepwise structure, and

a plurality of electrical vertical channels extending through the electrode stack in the direction that is normal to the top surface of the semiconductor layer, the plurality of electrical vertical channels electrically connected to the semiconductor layer; and

a first gap-fill layer surrounding a first connection plug that sequentially extends through the cell region and the peripheral region and is coupled to one electrical line of the plurality of electrical lines,

wherein the first gap-fill layer includes

a first dielectric layer filling a first portion of a first trench, the first trench having a depth that extends through the cell region and the peripheral region and approaches the one electrical line, the first dielectric layer having a top surface that is proximate to a top surface of the electrode stack;

a second dielectric layer filling a second portion of the first trench, the second dielectric layer having a top surface that is proximate to the top surface of the electrode stack, the top surface of the second dielectric layer being more recessed toward the semiconductor layer than the top surface of the first dielectric layer; and

a third dielectric layer filling a remaining portion of the first trench and covering the top surface of the second dielectric layer,

wherein the first dielectric layer has a U shape having two top ends on an inner sidewall surface of the first trench, the two top ends of the first dielectric layer adjacent to the top surface of the electrode stack,

the third dielectric layer further covers the two top ends of the first dielectric layer, and

the top surface of the first dielectric layer is located at a lower level than the top surface of the electrode stack.

429. The semiconductor device of claim 118, wherein

the first dielectric layer has ~~a~~ the U shape that defines an open enclosure that is open towards the top surface of the electrode stack, and

~~the U shape has two top ends on an inner sidewall surface of the trench,~~ the two top ends are more distal to a top surface of the ~~lower layer~~ semiconductor layer in relation to the recessed second dielectric layer and are isolated from direct contact with each other.

4310. The semiconductor device of claim 129, wherein

the second dielectric layer fills a portion of the open enclosure of the first dielectric

layer, and

the third dielectric layer is between the top ends of the first dielectric layer.

~~14~~11. The semiconductor device of claim ~~12~~9, wherein

the second dielectric layer fills a portion of the open enclosure of the first dielectric layer, and

the third dielectric layer is between and covers the top ends of the first dielectric layer.

~~15~~12. The semiconductor device of any one of claims ~~12-9~~ to ~~14~~11, wherein

the first dielectric layer includes a dielectric material having a density that is greater than a density of each of the second and third dielectric layers, and

the second and third dielectric layers have a same material composition.

~~16~~13. The semiconductor device of any one of claims ~~11-8~~ to ~~15~~12, wherein

the cell region is divided into a cell array region and an extension region,

the electrical vertical channels are on the cell array region,

the stepwise structure is on the extension region, and

the first connection plug is on the cell array region of the cell region and extends through the electrode stack.

~~17~~14. The semiconductor device of claim ~~16~~13, further comprising:

a second gap-fill layer surrounding a second connection plug that sequentially extends through the cell region and the peripheral region and is coupled to a separate electrical line of the plurality of electrical lines,

wherein the second connection plug is on the extension region of the cell region.

~~18~~15. The semiconductor device of claim ~~17~~14, wherein the second gap-fill layer includes a fourth dielectric layer filling a first portion of a second trench, the second trench having a depth that extends through the cell region and the peripheral region and approaches the separate electrical line, the fourth dielectric layer having a top surface that is proximate to a top surface of a dielectric layer;

a fifth dielectric layer filling a second portion of the second trench, the fifth dielectric layer having a top surface that is proximate to the top surface of the dielectric layer, the top surface of the fifth dielectric layer being more recessed toward the semiconductor layer than the top surface of the fourth dielectric layer; and

a sixth dielectric layer filling a remaining portion of the second trench and covering the top surface of the fifth dielectric layer.

~~19~~16. The semiconductor device of any one of claims ~~11-8~~ to ~~18~~15, wherein the electrode stack includes a plurality of electrodes that are stacked on the semiconductor layer and have pads at respective end portions of the electrodes, and the cell region further includes

a first connection line electrically connected to the first connection plug,

a plurality of dummy vertical channels extending through the stepwise structure,

a plurality of metal contacts coupled to separate, respective pads of the plurality of electrodes, and

a plurality of metal lines electrically connected to separate, respective metal contacts.

~~20~~17. The semiconductor device of any one of claims ~~11-8~~ to ~~19~~16, further comprising:

a plurality of first connection plugs, the plurality of first connection plugs including the first connection plug,

each first connection plug of the plurality of first connection plugs is between a separate pair of adjacent electrical vertical channels of the plurality of electrical vertical channels.