

Description

The invention relates to an attenuator circuit for attenuating an electric signal.

Such an attenuator circuit may be used in a frequency-to-phase converter of the type disclosed in United States Patent Specification US—A—3,763,436. In such a converter a pulse-shaped input signal is applied to one input of a comparator *via* a delay circuit and to the other input of said comparator *via* an attenuator circuit. On the output of the comparator a pulse-shaped output signal appears, whose pulses have all been subjected to exactly equal time delays. The attenuator circuit in the known circuit arrangement is a resistive voltage divider. In order to preclude harmonic distortion when such a frequency-to-phase converter is used in, for example, a demodulation device of a single-chip integrated FM-receiver as described in Electronics, Jan. 27, pages 129—130, the relationship between the frequency and phase must be substantially linear in the phase range from 0° to 180°. This relationship is found to be highly linear for very small attenuations of the input signal. Therefore, the attenuator circuit should provide a very accurate attenuation of the input signal. Therefore, the attenuator circuit should provide a very accurate attenuation of the input signal.

In such circuits the input signal is generally applied with a d.c. level different from zero, so that the use of a voltage divider results in a difference between the d.c. level of the attenuated signal and the d.c. level of the signal applied to the delay circuit. It is desirable to maintain these levels equal, which may be achieved by the use of a level-shifting circuit or, as is described in said United States Patent Specification, by applying the input signal to the attenuator circuit and the delay circuit *via* blocking capacitors. However, the blocking capacitors cannot be integrated. This renders the known attenuator circuit less suitable for integration in a fully integrated FM receiver, whose numbers of connection pins and external components have been minimized in order to minimize the dimensions.

It is an object of the invention to provide an attenuator circuit which provides an accurate attenuation, the d.c. level of the attenuated signal being substantially equal to that of the unattenuated signal. It is another object of the invention to provide an attenuator circuit which can be integrated completely.

To this end an attenuator circuit of a type as mentioned in the opening sentence is characterized in that it comprises a first and a second transistor, which each have a control terminal, a first main terminal and a second main terminal, which control terminals are coupled to input terminals for applying the input signal, which first main terminals have a common connection which is coupled to a first supply-voltage terminal *via* a current source and which second main terminals are each coupled to a second supply-voltage terminal *via* a respective load, two ends of a

voltage divider having two unequal resistors being coupled to the second main terminals, one of the ends of the voltage divider forms a first output for taking off the unattenuated output signal and the junction point of the resistors from a second output for taking off the attenuated output signal. (The control terminal, the first main terminal and the second main terminal are defined herein as the base electrode, emitter electrode and collector electrode respectively in case of bipolar transistors and as the gate-electrode, source electrode and drain electrode respectively in case of field-effect transistors). In the case of a circuit equipped with bipolar transistors the signal to be processed is applied to, for example, the base of one transistor of the differential amplifier, the unattenuated signal being taken from one of the collectors and the attenuated signal from said voltage divider. The d.c. level of the attenuated signal is substantially equal to that of the unattenuated signal, because in the absence of a signal on the inputs of the differential amplifier no quiescent current flows in the voltage divider, so that the voltage on the collectors of the differential amplifier is equal to the voltage on the tapping of the voltage divider. The load resistors of the differential amplifier and the resistors of the voltage divider can be integrated within a very small area and can thus be fabricated with a comparatively high accuracy, so that a very accurate voltage divider can be obtained.

It is noted, that the US—PS 4,105,942 discloses a circuit, a part of which shows some resemblance with the circuit according to the invention of this application. The known circuit, however, is related to an amplifier circuit, which is provided with a compensation for common mode offset voltages between the outputs of the amplifier and therefore is in no way related to an attenuator circuit for attenuating an electric signal.

An attenuator circuit in accordance with the invention may be further characterised in that one of the second main terminals and the tapping of the voltage divider are coupled to the control electrodes of a third and a fourth transistor respectively, which transistors are arranged as emitter followers. The attenuated and unattenuated signals are then available on low-impedance points, which may be coupled to further stages of the circuit.

Current sources may be arranged in the emitter lines of the third and the fourth transistor the ratio between the currents supplied by said sources being such that the d.c. level on the tapping for the attenuated signal is substantially equal to the d.c. level on the second main terminal which carries the unattenuated signal. The base currents of the third and fourth transistor influence the d.c. levels of the attenuated signal and the unattenuated signal. By a suitable choice of the currents supplied by the current sources in the emitter lines of the third and the fourth transistor the d.c. level on the base of the third transistor can be made equal to that on the base of the fourth transistor.

The ratio between the emitter areas of the third

and the fourth transistor may be substantially equal to the ratio between the currents in the emitter lines of the third and the fourth transistor. This step ensures that the base-emitter voltages of the third and the fourth transistor are equal, so that the d.c. levels of the attenuated signal and the unattenuated signal on the emitters of the third and fourth transistor are equal.

As an alternative a resistor may be arranged in at least one of the base lines of the third and the fourth transistor, which resistor has such a value that the d.c. level on the emitter of the third transistor is substantially equal to the d.c. level on the emitter of the fourth transistor. In this case the d.c. levels on the emitters of the third and the fourth transistors are not made equal by means of the currents from the current sources in the emitter lines of the third and the fourth transistors but by means of a resistor in at least one of the base lines. The currents supplied by the current sources in the emitter lines may then be equal or unequal. Moreover, the emitter area of the third and the fourth transistor may be equal or unequal.

The invention will now be described in more detail, by way of example, with reference to the accompanying drawing, in which

Figure 1 shows a frequency-to-phase converter equipped with an attenuator circuit in accordance with the invention,

Figure 2 shows some signal waveform appearing in the circuit shown in Figure 1.

Figure 1 shows a frequency-to-phase converter which is equipped with an attenuator circuit 1 in accordance with the invention, a delay circuit 2 and a comparator 3. The attenuator circuit 1 comprises two transistors T_1 and T_2 which are arranged as a differential pair, whose collectors are each connected to the positive supply-voltage terminal 5 via a respective resistor R_1 , and whose common emitter connection is connected to the earth terminal 6 via a current source 7 supplying a current of the value I_1 . In the present Application a current source is to be understood to mean a current-supply element having a high impedance. It is obvious that instead of resistors R_1 current sources, diodes etc. may be used as collector loads. The base of transistor T_1 is connected to the input terminal 4 and by means of a reference-voltage source 8 to the earth terminal 6. The base of transistor T_2 is also connected to the earth terminal 6 by means of a reference-voltage source 8. Between the collectors 9 and 10 of the transistors T_1 and T_2 a voltage divider is arranged, which comprises the resistors R_x and R_y . It is obvious that further circuit elements, such as emitter followers, may be arranged between the ends of the voltage divider and the collectors. These resistors have resistance values $R_x = R_2(1 + a)$ and $R_y = R_2(1 - a)$ respectively, a being a constant with a value $0 < a < 1$. The collector 9 of transistor T_2 is connected to the base of an emitter-follower transistor T_3 , a current source 12 supplying a current I_3 being arranged in the emitter line. Similarly, the tapping 11 of the

voltage divider R_x, R_y is connected to the base of an emitter-follower transistor T_4 , a current source 13 applying a current I_2 being arranged in the emitter line.

If no input signal appears on terminal 4 the current I_1 is divided uniformly between the transistors T_1 and T_2 , so that the voltage produced on points 9 and 11 by these currents are equal. The base current of transistor T_4 on point 11 is divided between the resistors R_1, R_x and R_y, R_1 and the base current of transistor T_3 on point 9 is divided between the resistors R_1 and R_y, R_x and R_1 . In order to ensure that these base currents do not cause a voltage difference between points 9 and 11 these base currents must have specific values. In the case of equal current-gain factors of the transistors T_3 and T_4 a simple calculation will show that the ratio between the currents from the current sources 12 and 13 should comply with:

$$\frac{I_3}{I_2} = 1 + \frac{R_2}{R_1} (1 + a).$$

Moreover, the base-emitter voltage of the transistors T_3 and T_4 must be equal to each other to ensure that the d.c. level on the emitter of transistor T_3 is accurately equal to that on the emitter of transistor T_4 . For this purpose the emitter areas A_3 and A_4 of the transistor T_3 and T_4 must be selected so that:

$$I_2/T_3 = A_4/A_3.$$

In another embodiment, not shown, the currents may be selected so that $I_2 = I_3$ and the emitter areas may be selected so that $A_3 = A_4$. The resulting voltage difference between points 9 and 11 is then compensated for by arranging a resistor in the base line of transistor T_4 , so that the d.c. level on the base of transistor T_3 is again equal to that on the base of transistor T_4 . Alternatively, the currents I_2 and I_3 and the emitter areas A_3 and A_4 may be selected to be unequal. Equal voltages on the emitters of the transistors T_3 and T_4 can then be obtained by arranging a resistor both in the base line of transistor T_3 and that of transistor T_4 .

By applying a pulse-shaped signal, for example, a frequency-modulated signal, to the input terminal 4 transistors T_1 and T_2 are alternately turned on and turned off, so that the polarity of the voltage difference between the collectors 9 and 10 changes each time. The amplified input signal appears on collector 9 of transistor T_2 and consequently on the emitter of transistor T_3 . Figure 2a shows the signal V_1 of the pulse height ΔV_1 on the emitter of transistor T_3 . The attenuated signal is taken from tapping 11. As a result of the inequality of the resistors $R_y = R_1(1 - a)$ and $R_x = R_2(1 + a)$, the signal voltage on tapping 11 follows the polarity of the voltage difference ΔV_1 between the collectors 9 and 10. The signal voltage V_2 on the tapping 11 and hence on the emitter of transistor T_4 has a pulse height

$$\Delta V_2 = \frac{(1+a)}{2} \Delta V_1.$$

Figure 2b shows this voltage V_2 . In order to obtain a substantially linear frequency-to-phase characteristic a low attenuation of the signal on the collector 9 of transistor T_2 is required. This low attenuation is obtained when the factor a is large, which factor has a value of approximately 0.8 to 0.9 in practice. Therefore, the resistors R_x and R_y and the resistors R_1 should have a very high relative accuracy in view of the offset compensation. Since in an integrated circuit these resistors can be arranged close to each other within a small area, these resistors can be fabricated with a minimal spread.

It is to be noted that the pulse-shaped input signal may be applied to the base of T_2 instead of to the base of T_1 , the signals on the collector 9 and the tapping 11 then being inverted. Alternatively, the positive pulse half may be applied to the base of T_1 and the negative pulse half to the base of T_2 .

The signal on the emitter of transistor T_3 is applied to the base of transistor T_5 , which forms part of a delay circuit 2, the attenuated signal on the emitter of transistor T_4 being applied to the first input 20 of the comparator 3.

The delay circuit 2, of which a simple version is shown for the sake of clarity, comprises two transistors T_5 and T_6 which are arranged as a differential pair and whose common emitter connection is coupled to the earth terminal 6 by means of a current source 14 supplying a current I_4 . The differential pair T_5 , T_6 is loaded by a current mirror, which in the present embodiment comprises a transistor T_7 , arranged as a diode, and a transistor T_8 , which transistors have common-ned base-s. The emitters of the transistors T_7 and T_8 are coupled to the positive supply-voltage terminal 5 via resistors R_7 and R_8 respectively. A capacitor C_1 is coupled to the output and in the present example it is connected to the positive supply-voltage terminal 5. The capacitor C_1 is added externally to the integrated circuit. Moreover, the output is connected to the base of an emitter-follower transistor T_9 , a current source 15 supplying a current I_5 being arranged in the emitter line. The emitter of transistor T_9 is coupled to the base of transistor T_6 and to the input 21 of the comparator 3. The ratio between resistors R_7 and R_8 is selected so that the collector currents of the transistors T_5 and T_6 are substantially equal to each other.

In the absence of an input signal on the base of transistor T_5 , capacitor C_1 is charged so far that the d.c. level on the base of transistor T_6 is equal to that of transistor T_5 . Consequently, the d.c. levels on the inputs 20 and 21 are also equal, so that no signal appears on output 22 of the comparator 3.

If the pulse-shaped input signal V_1 appears on the base of transistor T_5 , transistors T_5 and T_6 conduct alternately, so that capacitor C_1 is charged and discharged respectively. Capacitor

C_1 is charged until the voltage across the capacitor and via emitter follower T_9 , the voltage on the base of transistor T_6 is equal to the maximum value of the voltage V_1 on the base of transistor T_5 . Similarly, during discharging the voltage on the base of transistor T_6 decreases until it is equal to the minimum value of the voltage V_1 on the base of transistor T_5 . In Fig 2b V_3 represents the voltage variation on the emitter of transistor T_9 and hence on input 21 of the comparator 3. The voltages V_2 and V_3 shown in Fig. 2b are the input voltages of the comparator 3. The comparator 3 compares these voltages and the voltage level on the output 22 of comparator 3 changes each time that the polarity of the voltage difference changes. Figure 2c shows the variation of this voltage V_4 . The pulses on the output 22 have all been delayed by substantially the same time T for a wide frequency range, so that a substantially linear relationship is obtained between the frequency and phase in the range from 0 to 180°. The frequency for which the output signal lags the phase of the input signal by 90° is called the characteristic frequency f_0 . The time t_0 corresponding to this frequency f_0 is equal to the time necessary for the capacitor C_1 to be charged by such an amount that the voltage variation across the capacitor C_1 is equal to ΔV_1 , or

$$t_0 = \frac{\Delta V_1 \times C_1}{I_4}.$$

If this time t_0 must be temperature-independent both ΔV_1 and I_4 must be temperature-independent. A temperature-independent voltage variation ΔV_1 can be obtained by applying a signal to the input terminal 4, which signal is derived with the aid of a temperature-independent band-gap voltage, and by using for the current source 14 a current source of a type described in the simultaneously filed Patent Application (PHN. 10.630).

The invention has been described in the context of an embodiment comprising NPN-transistors and two PNP-transistors. It is obvious that the NPN-transistors may be replaced by PNP-transistors and the PNP-transistors by NPN-transistors. Alternatively, field-effect transistors may be employed.

Claims

1. An attenuator circuit for converting an input signal into an unattenuated output signal and an attenuated output signal, characterized in that it comprises a first and a second transistor, which each have a control terminal, a first main terminal and a second main terminal, which control terminals are coupled to input terminals for applying the input signal, which first main terminals have a common connection, which is coupled to a first supply-voltage terminal via a current source and which second main terminals are each coupled to a second supply-voltage terminal via a respective load, two ends of a voltage divider having two

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unequal resistors being coupled to the second main terminals, one of the ends of the voltage divider forms a first output for taking off the unattenuated output signal and the junction point of the resistors forms a second output for taking off the attenuated output signal.

2. An attenuator circuit as claimed in Claim 1, characterized in that one of the second main terminals and the tapping of the voltage divider are coupled to the control electrodes of a third and a fourth transistor respectively, which transistors are arranged as emitter followers.

3. An attenuator circuit as claimed in Claim 2, characterized in that current sources are arranged in the emitter lines of the third and fourth transistor, the ratio between the currents supplied by said sources being such that the d.c. level on the tapping for the attenuated signal is substantially equal to the d.c. level on the second main terminal which carries the unattenuated signal.

4. An attenuator circuit as claimed in Claim 3, characterized in that the ratio between the emitter areas of the third and the fourth transistor is substantially equal to the ratio between the currents in the emitter lines of the third and fourth transistor.

5. An attenuator circuit as claimed in Claim 2, characterized in that a resistor is arranged in at least one of the base lines of the third and the fourth transistor, which resistor has such a value that the d.c. level on the emitter of the third transistor is substantially equal to the d.c. level on the emitter of the fourth transistor.

Patentansprüche

1. Abschwächungsschaltung zum Umsetzen eines Eingangssignals in ein nicht abgeschwächtes Ausgangssignal und ein abgeschwächtes Ausgangssignal, dadurch gekennzeichnet, dass darin ein erster und ein zweiter Transistor vorgesehen sind, die je einen Steueranschluss, einen ersten Hauptanschluss und einen zweiten Hauptanschluss haben, wobei die Steueranschlüsse mit Eingangsschlüssen zum Anlegen des Eingangssignals verbunden sind, wobei die ersten Hauptanschlüsse eine gemeinsame Verbindung haben, die mit einem ersten Speisespannungsanschluss über eine Stromquelle gekoppelt ist und die zweiten Hauptanschlüsse mit je einem zweiten Speisespannungsanschluss über eine jeweilige Belastung gekoppelt sind, wobei zwei Ende eines Spannungsteilers mit zwei ungleichen Widerständen an die zweiten Hauptanschlüsse gekoppelt sind, wobei eines der Ende des Spannungsteilers einen ersten Ausgang zum Abnehmen des ungeschwächten Ausgangssignals bildet und der Knotenpunkt der Widerstände einen zweiten Ausgang zum Abnehmen des abgeschwächten Ausgangssignals bildet.

2. Abschwächungsschaltung nach Anspruch 1, dadurch gekennzeichnet, dass einer der zweiten Hauptanschlüsse und die Abzweigung des Spannungsteilers mit den Steuerelektroden eines

dritten bzw. eines vierten Transistors gekoppelt sind wobei diese Transistoren als Emitterfolger angeordnet sind.

3. Abschwächungsschaltung nach Anspruch 2, dadurch gekennzeichnet, dass Stromquellen in die Emitterleitungen der dritten und vierten Transistoren aufgenommen sind, wobei das Verhältnis zwischen den von diesen Quellen gelieferten Strömen derart ist, dass der Gleichspannungspegel an der Abzweigung für das abgeschwächte Signal im wesentlichen gleich dem Gleichspannungspegel am zweiten Hauptanschluss ist, der das unabgeschwächte Signal führt.

4. Abschwächungsschaltung nach Anspruch 3, dadurch gekennzeichnet, dass das Verhältnis zwischen den Emitterbereichen des dritten und vierten Transistors im wesentlichen gleich dem Verhältnis zwischen den Strömen in den Emitterleitungen des dritten und vierten Transistors ist.

5. Abschwächungsschaltung nach Anspruch 2, dadurch gekennzeichnet, dass ein Widerstand in zumindest eine der Basisleitungen des dritten und vierten Transistors aufgenommen ist wobei dieser Widerstand einen derartigen Wert hat, dass der Gleichspannungspegel am Emitter des dritten Transistors im wesentlichen gleich dem Gleichspannungspegel des Emitters der vierten Transistors ist.

Revendications

1. Circuit atténuateur servant à convertir un signal d'entrée en un signal de sortie non atténué et un signal de sortie atténué, caractérisé en ce qu'il comporte un premier et un deuxième transistor, qui sont munis chacun d'une borne de commande, d'une première borne principale et d'une seconde borne principale, ces bornes de commande étant couplées à une borne d'entrée pour l'application du signal d'entrée, les premières bornes principales présentant une connexion commune qui est couplée à une première borne de tension d'alimentation par l'intermédiaire d'une source de courant, les secondes bornes principales étant couplées chacune à une deuxième borne de tension d'alimentation par l'intermédiaire d'une charge respective, deux extrémités d'un diviseur de tension présentant deux résistances non égales étant couplées aux deuxième bornes principales, l'une des extrémités du diviseur de tension formant une première sortie pour le prélèvement du signal de sortie non atténué, et le point de jonction des résistances formant une deuxième sortie pour le prélèvement du signal de sortie atténué.

2. Circuit atténuateur selon la revendication 1, caractérisé en ce que l'une des deuxième bornes principales et la prise du diviseur de tension sont couplées aux électrodes de commande d'un troisième transistor et d'un quatrième transistor respectivement, transistors qui sont montés comme émetteurs suiveurs.

3. Circuit atténuateur selon la revendication 2, caractérisé en ce que des sources de courant sont



montées dans les lignes émettrices des troisième et quatrième transistors, le rapport entre les courants fournis par lesdites sources étant tel que le niveau de tension continue à la prise pour le signal atténué soit pratiquement égal au niveau de tension continue à la deuxième borne principale qui présente le signal non atténué.

4. Circuit atténuateur selon la revendication 3, caractérisé en ce que le rapport entre les zones d'émetteur des troisième et quatrième transistors est pratiquement égal au rapport entre les cou-

rants dans les lignes émettrices des troisième et quatrième transistors.

5. Circuit atténuateur selon la revendication 2, caractérisé en ce qu'une résistance est insérée dans au moins l'une des lignes de base des troisième et quatrième transistors, résistance qui présente une valeur telle que le niveau de tension continue à l'émetteur du troisième transistor est pratiquement égal au niveau de tension continue à l'émetteur du quatrième transistor.

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