

APPARATUS AND METHOD FOR TESTING INTEGRATED CIRCUITS
ABSTRACT OF THE DISCLOSURE

A testing methodology for very large scale integrated circuits, for example, microprocessors having several million transistors. Initially a set of pseudorandom test patterns is selected. During the design of the integrated circuit it is partitioned into functional units and each unit is designed to be verified and tested by the test patterns. During a test mode all of the units of the integrated circuit receives the test patterns in parallel. The output from each unit is coupled to a signature register. The contents of the signature registers are examined following application of the test pattern. This testing methodology lends itself to the simultaneous testing of many integrated circuits.

Figure 1