162162
G00002

ABSTRACT

ISOLATION STRUCTURE FOR A MEMORY CELL USING Al_2O_3 DIELECTRIC

The invention provides, in one exemplary embodiment, an isolation gate formed over a substrate for biasing the substrate and providing isolation between adjacent active areas of an integrated circuit structure, for example a DRAM memory cell. An aluminum oxide (Al_2O_3) is used as a gate dielectric, rather than a conventional gate oxide layer, to create a hole-rich accumulation region under and near the trench isolation region. Another exemplary embodiment of the invention provides an aluminum oxide layer utilized as a liner in a shallow trench isolation (STI) region to increase the effectiveness of the isolation region. The embodiments may also be used together at an isolation region.

FIG. 2A