

ABSTRACT

PROGRAMMABLE DIVIDER

A programmable divider circuit (10) for dividing a binary number F . A plurality of multiplexer arrays (26, 66, 83, 86, 92, 98) produce a selected one of either zero or F shifted by 1 to $N-1$ bits where N is the number of bits making up F . A plurality of adder arrays (44, 84, 88, 94, 96) selectively add the shifted values of F to produce the desired division.

Figure 1