CLAIMS

1. A semiconductor memory device comprising:

a NAND string;

a first storage unit configured to store:

a first unique number uniquely assigned; and

a first chip address having a bit number smaller than that of the first unique number and used to identify semiconductor memory devices; and

a first determination unit configured to externally receive a first command set that includes a second unique number, and to write a second chip address included in the first command set to the first storage unit as the first chip address when the second unique number matches the first unique number.

2. The semiconductor memory device according to claim 1, further comprising:

if a second command set that includes a third chip address is externally received, and

if it is determined that the third chip address matches the first chip address stored in the first storage unit,

a second determination unit configured to cause a command included in the second command set to be executed.

3. The semiconductor memory device according to claim 1, wherein

the device is enabled when a first signal is externally received.

4. A memory system, comprising:

a first package comprising a first memory chip and a second memory chip;

a controller configured to control the first package; and

a bus that electrically connects the controller to the first package,

wherein:

the first memory chip and the second memory chip are obliquely stacked,

the first memory chip and the second memory chip each have a group of pads for receiving a signal or a voltage from the bus, and the groups of pads of the first memory chip and the second memory chip are connected in common to each other,

the first memory chip and the second memory chip each have a first unique number that is uniquely assigned to the memory chip and a first chip address having a bit number smaller than that of the first unique number and used to identify the memory chip from other memory chips,

the controller is configured to supply a first command set that includes a second unique number and a second chip address to the memory chips, and

the first memory chip and the second memory chip each store the second chip address as the first chip address when the second unique number matches the first unique number.

5. The memory system according to claim 4, wherein

the controller supplies a second command set that includes a third chip address to the first memory chip and the second memory chip,

the first memory chip and the second memory chip execute a command that is included in the second command set when it is determined that the third chip address matches the first chip address.

6. The memory system according to claim 4, wherein

the first memory chip and the second memory chip each control an operation timing based on the first chip address.

7. The memory system according to claim 4, further comprising:

a second package comprising a third memory chip and a fourth memory chip, wherein

the third memory chip and the fourth memory chip each have a group of pads for receiving a signal or a voltage from the bus, and the groups of pads of the first to fourth memory chips are connected in common to each other,

the third memory chip and the fourth memory chip each have a first unique number that is uniquely assigned to the memory chip and a first chip address having a bit number smaller than that of the first unique number and used to distinguish the memory chip from other memory chips.