METHOD FOR MAKING AN INTEGRATED CIRCUIT HAVING A DUMMY STRUCTURE

Abstract of the Disclosure

A pattern of dummy structures (20) is added to the layout pattern of an integrated circuit (10) to equilibrate the polishing rate across the surface of a semiconductor substrate (11). The location of each dummy structure (20) is predetermined so that it does not intersect a well boundary (17) or an active region (21,27), and does not fall under a conductive material such as a layer of polysilicon (22,28) or an interconnect structure (23,29).

Fig. 1 accompanies the abstract.