

MICROFEATURE WORKPIECE SUBSTRATES HAVING THROUGH-SUBSTRATE VIAS, AND ASSOCIATED METHODS OF FORMATION

TECHNICAL FIELD

[0001] The present invention is directed generally toward microfeature workpiece substrates having through-substrate vias, and associated methods of formation.

BACKGROUND

[0002] Packaged microelectronic assemblies, such as memory chips and microprocessor chips, typically include a microelectronic die mounted to a substrate (e.g., an interposer board) and encased in a plastic protective covering. The die includes functional features, such as memory cells, processor circuits, and interconnecting circuitry. The die also typically includes die bond pads that are electrically coupled to the functional features. The bond pads are coupled to corresponding first bond pads on the substrate (e.g., with wirebonds), and this connection is protected with the plastic protective covering. The first substrate bond pads can be coupled to second substrate bond pads on an opposite surface of the substrate via pathways that are internal to the substrate. The second bond pads can in turn be connected to external devices, for example, using solder balls. Accordingly, the substrate can have one or more layers of conductive material (e.g., copper) that is etched or otherwise configured to form the first substrate bond pads and the second substrate bond pads.

[0003] In a typical operation, the substrate bond pads are built up in an electrolytic plating operation using a bus formed from the conductive layers to transmit electrical current to the bond pads. One drawback with the bus is that it can act as an antenna and can accordingly create extraneous signals, which may interfere with the operation of the microelectronic die. Accordingly, several techniques have been developed for forming bond pads on a substrate without requiring that a bus remain in the substrate. While these techniques have met with at least some success, they have also been subject to

several drawbacks. These drawbacks can include undercutting the conductive material at the bond pads and/or difficulty in obtaining very fine pitch spacing between adjacent bond pads. As the size of microelectronic dies continues to decrease, and performance demands on the microelectronic dies continues to increase, these drawbacks can in some cases place undesirable design and/or performance limitations on the microelectronic dies.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Figures 1A-1F illustrate an initial series of steps for forming a substrate without a permanent bus, in accordance with an embodiment of the invention.

[0005] Figures 2A-2D illustrate subsequent steps for forming the substrate initially shown in Figures 1A-1F.

[0006] Figure 3 is an enlarged illustration of a portion of a substrate configured in accordance with an embodiment of the invention, shown coupled to a microfeature workpiece and an external device.

[0007] Figure 4 illustrates a packaged microelectronic device having a substrate coupled to an external device in accordance with an embodiment of the invention.

[0008] Figure 5 illustrates a packaged microelectronic device having a substrate coupled to an external device in accordance with another embodiment of the invention.

DETAILED DESCRIPTION

A. Introduction

[0009] Microfeature workpiece substrates having through-substrate vias, and associated methods of formation are described below. In particular aspects, the through-substrate vias can allow the formation of bond pads on one surface without requiring a bus at that surface. Instead, electrical current for forming the bond pads in an electrolytic process can be provided by a conductive path that extends through the via. A method for forming a support substrate for carrying microfeature dies in accordance with one aspect of the invention includes exposing a substrate to an electrolyte, wherein the substrate has

a first side with a first conductive layer, a second side opposite the first side with a second conductive layer, and a conductive path extending through the substrate from the first conductive layer to the second conductive layer. The method can further include forming a bond pad at a bond site of the first conductive layer by disposing at least one conductive bond pad material at the bond site. The process of disposing the at least one conductive bond pad material can include passing an electrical current between the first and second conductive layers via the conductive path, while the substrate is exposed to the electrolyte.

[0010] In further particular aspects, the method can include patterning the first conductive layer to form a bond site, and applying bond pad material to the bond site after patterning the first conductive layer. In still another aspect, the method can include applying an at least generally non-removable protective coating over the first conductive layer, preventing the protective coating from covering the bond site (or removing the protective coating from the bond site) and applying bond pad material to the bond site after applying the protective coating.

[0011] In yet another aspect, the method can include forming a bond pad at a first bond site of the first conductive layer and at a second bond site of the second conductive layer. This process can further include (a) placing a removable protective coating over the second conductive layer, (b) preventing the removable protective coating from covering the second bond site or removing the protective coating from the second bond site, and (c) applying conductive material to the first and second bond sites simultaneously, after performing processes (a) and (b). The method can still further include (d) removing the removable protective coating from the second conductive layer, and (e) patterning the second conductive layer by removing a portion of the second conductive layer while leaving the second bond site electrically coupled to the first bond site via the conductive path.

[0012] In still further aspects, the invention can include a microelectronic system comprising a substrate configured to carry a microfeature die, with the substrate having a first surface with a first conductive layer and a second surface facing opposite from the first surface and having a second conductive layer. The first conductive layer can have multiple first bond sites, and the second conductive layer can have multiple second bond

sites. The system can further comprise conductive bond pad material positioned at the first bond sites to form first bond pads, with the first bond pads being separated from each other by a first average spacing, and with the bond pad material extending around an edge of the first conductive layer at the first bond sites. Conductive bond pad material can also be positioned at the second bond sites to form second bond pads, with the first and second bond pads being electrically coupled with conductive pathways extending through the substrate. The second bond pads can be separated from each other by a second average spacing greater than the first average spacing. The bond pad material can have a different arrangement at the second bond sites than at the first bond sites. For example, the bond pad material at the second bond site can be spaced apart from an edge of the second conductive layer at the second bond sites.

[0013] As used herein, the terms "microfeature workpiece" and "workpiece" refer to substrates on and/or in which microelectronic devices are integrally formed. Typical microelectronic devices include microelectronic circuits or components, thin-film recording heads, data storage elements, microfluidic devices and other products. Micromachines and micromechanical devices are included within this definition because they are manufactured using much of the same technology that is used in the fabrication of integrated circuits. The microfeature workpiece can be a semiconductive piece (e.g., doped silicon wafers or gallium arsenide wafers) nonconductive pieces (e.g., various ceramic substrates) or conductive pieces. In some cases, the workpieces are generally round, and in other cases, the workpieces have other shapes, including rectilinear shapes.

[0014] The term "support substrate" is used generally herein to refer to a support member that carries the microfeature workpiece and provides an interface between the microfeature workpiece and external devices to which the microfeature workpiece may be electrically coupled. Accordingly, the term "support substrate" can include, but is not limited to, interposer boards, printed circuit boards, and/or other structures that can provide physical support and/or electrical connections for the microfeature workpiece and that generally do not include integrated semiconductor features.

B. Support Substrates and Associated Methods of Formation

[0015] Figures 1A-2D illustrate a series of process steps that may be performed to produce a support substrate having features in accordance with several embodiments of the invention. Referring first to Figure 1A, the support substrate 110 can include a core material 113 having a first side or surface 111a and a second side or surface 111b facing opposite from the first surface 111a. A first conductive layer 112a can be positioned against the first surface 111a, and a second conductive layer 112b can be positioned against the second surface 111b. The substrate 110 can include a printed circuit board, with the core 113 including a ceramic material, and the first and second conductive layers 112a, 112b including generally planar layers of copper. In other embodiments, these components can have different compositions and/or arrangements.

[0016] Referring next to Figure 1B, a via 114 can be formed to extend through the core 113 and through the first and second conductive layers 112a, 112b. As shown in Figure 1C, the via 114 can be coated with a third conductive layer 112c to form a conductive path 115 that electrically connects the first conductive layer 112a and the second conductive layer 112b. The third conductive layer 112c can be formed using a conventional combination of electroless and electrolytic plating techniques. For example, an electroless technique can be used to apply a seed layer to the walls of the via 114, and an electrolytic technique can be used to add thickness to the seed layer, forming the overall structure of the third conductive layer 112c.

[0017] In Figure 1D, the first conductive layer 112a can be patterned to remove the bulk of the first conductive layer 112a, with the exception of at least one first bond site 130a located adjacent to the first surface 111a of the core material 113. For purposes of illustration, only one first bond site 130a is shown in Figures 1D-2D and described in the associated text. However, it will be understood by those of ordinary skill in the art that the support substrate 110 can include additional first bond sites 130a at other locations, within and/or transverse to the plane of Figure 1D. In any of these embodiments, for at least some of the first bond sites 130a, no electrical connection exists between the first bond site 130a and other first bond sites located at the first surface 111a after the patterning process has been completed. In particular, each first bond site 130a can be electrically

independent of other features at the first surface 111a. Accordingly, the first conductive layer 112a need not include an electrically conductive bus. Instead, as will be described later, electrical current for carrying out manufacturing processes at the first bond site 130a can be provided by the second conductive layer 112b and the conductive path 115.

[0018] The first bond site 130a can be formed using any of a variety of conventional patterning techniques. Such techniques can include disposing a layer of photoresist or another protective coating on the first conductive layer 112a, patterning the photoresist to remove portions of the photoresist over portions of the first conductive layer 112a that do not correspond to the first bond site 130a, and then exposing the first conductive layer 112a to an etchant that removes all or generally all of the first conductive layer 112a except at the location corresponding to the first bond site 130a.

[0019] Referring next to Figure 1E, a first protective coating 140a can be disposed over the first surface 111a and the first conductive layer 112a, except over the first bond site 130a. In a particular aspect of this embodiment, the first protective coating 140a can include a soldermask or other material that remains permanently attached to the support substrate 110 after processing. For example, the first protective coating 140a can include a soldermask material that is patterned in a manner generally similar to that described above with reference to Figure 1D, but which is then treated (e.g., by exposure to radiation, heat, or another energy source) to form a generally permanent coating. As used herein, the term "at least generally permanent" refers to a material that remains with the support substrate 110 after processing, and that is not removed (or at least not entirely removed) during the manufacturing process and/or prior to coupling the support substrate 110 to a microfeature die or other device for an end-user.

[0020] As is also shown in Figure 1E, the first protective coating 140a can be applied so that a gap 117 exists between a first conductive layer edge 116a and the first protective coating 140a. As described in greater detail below with reference to Figure 2A, the gap 117 can allow for a more extensive application of bond pad material at the first bond site 130a.

[0021] Referring next to Figure 1F, a second protective coating 140b can be applied to the second conductive layer 112b. The second protective coating 140b can be patterned in a manner generally similar to that described above to expose or keep exposed a second bond site 130b. Unlike the first protective coating 140a, however, the second protective coating 140b can be completely removed during subsequent processing steps. Accordingly, the second protective coating 140b can include a dry film or other patternable, removable material. For purposes of illustration, the second bond site 130b is shown more or less directly beneath the first bond site 130a; however, in many cases, the second bond site 130b can be positioned further away from the via 114. This can result in larger spacings (e.g., coarser pitch) between adjacent second bond sites 130b than between adjacent first bond sites 130a.

[0022] Figures 2A-2D illustrate process steps for providing additional conductive material at the first bond site 130a and the second bond site 130b (referred to collectively as bond sites 130). The additional conductive material applied to the bond sites 130 can provide for enhanced electrical connectivity between the bond sites 130 and the structures to which the bond sites are electrically coupled. In the case of the first bond site 130a, the coupling can be to a microelectronic die that the support substrate 110 carries and is packaged with. In the case of the second bond site 130b, the connection can be to an external device.

[0023] Beginning with Figure 2A, the support substrate 110 can be disposed in an electrolyte 118, and a cathode 119 can be applied to the second conductive layer 112b. One or more anodes 120 can be positioned in electrical communication with the electrolyte 118 to complete the electrical circuit used for electrolytically applying material to the first bond sites 130. The differences in electrical potential between the anode 120 and cathode 119 provides for the current flow. At this point, the second conductive layer 112b can be generally continuous over the second surface 111b of the support substrate 110, with the exception of local discontinuities at the vias 114. Accordingly, the second conductive layer 112b can provide a highly conductive, low resistance link to the second bond site 130b. The second conductive layer 112b can also provide a highly conductive,

low resistance link to the first bond site 130a, via the conductive path 115 formed by the third conductive layer 112c extending through the via 114.

[0024] During the electrolytic process, a first bond pad material 131a can be applied to the first bond site 130a and can form a first bond pad 137a. A second bond pad material 131b can be applied to the second bond site 130b to form a second bond pad 137b. The first and second bond pad materials 131a, 131b are referred to collectively as bond pad material 131. The bond pad material 131 can include a single constituent or a composite of constituents. For example, in one embodiment, the bond pad material 131 can include both nickel and gold, arranged in layers with a nickel layer 135 placed adjacent to the underlying conductive layer 112a, 112b, and with a gold layer 136 positioned against the nickel layer 135. In other embodiments, the bond pad material 131 can include composites of different conductive materials, or a single layer of a homogenous material. In any of these embodiments, the first bond pad material 131a can at least partially fill the gap 117 between the first protective coating 140a and the edge 116 of the first conductive layer 112a. The presence of the gap 117 can allow the first bond pad material 131a to wrap around the edge 116a of the first conductive layer 112a. In particular, the first bond pad material 131a need not be offset away from the edge 116a of the first conductive layer 112a. This feature can be enabled by (a) patterning the first conductive layer 112a before applying the first bond pad material 131a, and (b) using a soldermask or similar material for the first protective coating 140a. As a result, the first bond site 130a can have a relatively large amount of first bond pad material 131a accessible for electrical coupling, even though the first bond site 130a itself may be relatively small to allow for close spacing between adjacent first bond sites 130a.

[0025] After the bond pad material 131 has been applied to the bond sites 130, the second protective coating 140b can be removed from the second surface 1116. Afterwards, the second conductive layer 112b can be patterned to remove conductive material other than that located at the second bond site 130b. Referring now to Figure 2B, a third protective coating 140c can be disposed over the second conductive layer 112b, and can then be patterned to protect the second bond site 130b and the conductive path 115 through the via 114. Accordingly, the third protective coating 140c can include a

temporary or otherwise removable, patternable material (e.g., a dry film, generally similar to the second protective coating 140b described above). In a particular aspect of this embodiment, the third protective coating 140c can extend around an edge 132 of the second bond pad material 131b to protect the entire volume of the second bond pad material 131b. As a result, the portion of the second conductive layer 112b of the second bond site 130b can be protected from being undercut when adjacent portions of the second conductive layer 112b are removed.

[0026] Referring next to Figure 2C, portions of the second conductive layer 112b surrounding the second bond site 130b can be removed (e.g., via an etching process), after which the third protective coating 140c itself can also be removed. The second bond site 130b can include an offset 133 between an edge 132 of the second bond pad material 131b, and an edge 116b of the second conductive material 112b. The formation of this offset 133 results from the fact that the third protective coating 140c was placed around the edge 132 during the process described above with reference to Figure 2B. This offset 133 can result in a slight increase in the overall size of the second bond site 130b (particularly in comparison to the first bond site 130a). However, this increase in size is not expected to create undesirable increases in the spacing between adjacent second bond sites 130b, because, on the second surface 112b of the substrate 110, bond site spacing is not as critical. In particular, the second bond sites 130b are intended to align with corresponding bond pads of external devices, which typically do not have bond pad pitch requirements as stringent as those for microfeature workpieces that are attached to the first bond sites 130a.

[0027] In Figure 2D, a fourth protective coating 140d is applied to the second surface 111b to provide for an at least generally permanent covering over the portions of the substrate 110 adjacent to the second bond site 130b. Accordingly, the fourth protective coating 140d can include a solder mask material that is either applied to (and then removed from) the second bond site 130b, or prevented from adhering to the second bond site 130b with an appropriate removable masking material. The support substrate 110 is now available for coupling to microfeature workpieces, and subsequently to external devices.

C. Support Substrates and Associated Installations

[0028] Figure 3 is an enlarged, partially schematic illustration of a portion of the substrate 110, coupled to both a microfeature workpiece 150 and an external device 160. In one aspect of this embodiment, the substrate 110 can be coupled to the microfeature workpiece 150 via a first conductive coupler 134a (e.g., a small solder ball) that extends between the first pad 137a and a corresponding bond pad 337a of the microfeature workpiece 150. The substrate 110 can be coupled to the external device 160 with a second conductive coupler 134b (e.g., a larger solder ball) that extends between the second bond pad 137b and a corresponding bond pad 337b of the external device 160. The external device 160 can include a printed circuitboard or other device that is in electrical communication with the microfeature workpiece 150 by virtue of the interposed substrate 110.

[0029] Figure 4 is an overall view illustrating the microfeature workpiece 150 positioned on the support substrate 110 and surrounded by an encapsulant 152 to form a packaged microelectronic device 151. This arrangement, typically referred to as a flip chip arrangement, includes a relatively fine pitch between the first bond pads 137a to accommodate the relatively close spacing of the corresponding bond pads 337a on the microfeature workpiece 150, and a coarser spacing of the second bond pads 137b. As discussed above, the second bond pads 137b typically need not be as closely spaced as the first bond pads 137a because the pitch requirements of the bond pads 337b on external device 160 are generally not as stringent as the pitch requirements of the microfeature workpiece 150.

[0030] In other embodiments, support substrates generally similar to those described above can be used in other arrangements. For example, referring now to Figure 5, a support substrate 510 can be configured to support a microfeature workpiece 550 in a chip-on-board (COB) arrangement. Accordingly, the microfeature workpiece 550 can be electrically coupled to the support substrate 510 with first conductive couplers 534a that include wirebonds extending between the first bond pads 137a of the support substrate 510, and corresponding bond sites 537a on an upper surface of the microfeature workpiece 550. Second conductive couplers 534b (which can include solder balls) can

extend between the second bond pads 137b and corresponding bond pads 537b of the external device 160. An encapsulant 552 can be positioned around the microfeature workpiece 550 and the support substrate 510 to form the packaged microelectronic device 551. In still other embodiments, the support substrate 510 can be configured to support microfeature workpieces in accordance with other configurations and/or arrangements.

[0031] One feature of embodiments of the support substrates and associated manufacturing methods described above is that the conductive bond pad material 131a can be applied to the first bond site 130a without the need for a bus at the first surface of the support substrate 110. Instead, electrical power for applying the first bond pad material 130a can be provided by applying current to the second conductive layer 112b and using the conductive path 115 provided by the via 114 to conduct electrical current to the first bond site 130a. An advantage of this arrangement is that the first bond pad 137a can be formed without a bus and accordingly, the potentially negative effects associated with a bus (e.g., extraneous signals that may result when the bus acts as an antenna), may be eliminated.

[0032] Another feature of embodiments of the support substrate described above is that the first bond pad material 131a can cover not only the outwardly facing surface of the first conductive material 112a at the first bond site 130a, but can also cover the adjacent edge 116. An advantage of this arrangement is that it can reduce or at least eliminate the likelihood that subsequent etching processes will undercut the first conductive layer 112a at the edge 116, by virtue of the protection afforded by the first bond pad material 131a at this location. As a result, the physical and electrical characteristics of the first bond pad 137a can be more robust than corresponding bond pads formed by other methods.

[0033] Another feature of embodiments of the support substrate described above is that the first bond material 131a is not offset from the edge of the first conductive layer 112a immediately below (unlike the second bond pad material 130b, which is offset from the edge of the corresponding second conductive layer 112b by an offset 133). An advantage of this arrangement is that it can provide for a greater surface area of highly conductive material at the first bond site 130a than would be available if the first bond pad material 131a were offset from the underlying first conductive layer 112a. This can allow

the overall size of the first bond site 130a to be reduced (because the available area at the first bond site 130a is more effectively utilized) and can accordingly allow adjacent first bond pads 137a to be spaced more closely together. An advantage of this arrangement is that it can allow for electrical connections (via solder balls or other structures) to corresponding microfeature workpieces that have very fine bond pad pitch spacings.

[0034] From the foregoing, it will be appreciated that specific embodiments of the invention have been described herein for purposes of illustration, but that various modifications may be made without deviating from the invention. For example, in some embodiments, the bond sites can have arrangements different than those described above. Many of the Figures illustrate features of the disclosed embodiments in a schematic fashion. Accordingly, many of these features may have dimensions and/or relative dimensions that are different than those illustrated in the Figures. Aspects of the invention described in the context of particular embodiments may be combined or eliminated in other embodiments. Further, while advantages associated with certain embodiments of the invention have been described in the context of those embodiments, other embodiments may also exhibit such advantages, and not all embodiments need necessarily exhibit such advantages to fall within the scope of the invention. Accordingly, the invention is not limited, except as by the appended claims.

CLAIMS

I/We claim:

[c1] 1. A method for forming a support substrate for carrying microfeature dies, comprising:

exposing a support substrate to an electrolyte, the support substrate having a first side with a first conductive layer, a second side opposite the first side with a second conductive layer, and a conductive path extending through the support substrate from the first conductive layer to the second conductive layer; and

forming a bond pad at a bond site of the first conductive layer by disposing at least one conductive bond pad material at the bond site, wherein disposing the at least one conductive bond pad material includes passing an electrical current between the first and second conductive layers via the conductive path while the support substrate is exposed to the electrolyte.

[c2] 2. The method of claim 1, further comprising forming a hole in the support substrate and disposing a conductive material in the hole to connect the first and second conductive layers.

[c3] 3. The method of claim 1, further comprising applying an electrical potential directly to the second conductive layer without applying the electrical potential directly to the first conductive layer, other than through the conductive path.

[c4] 4. The method of claim 1, further comprising applying an electrical potential to the second conductive layer while the second conductive layer covers at least approximately the entire second side.

[c5] 5. The method of claim 1, further comprising applying an electrical potential to the second conductive layer prior to patterning the second conductive layer to form bond pads at the second conductive layer.

[c6] 6. The method of claim 1, further comprising patterning the first conductive layer to remove conductive material adjacent to the bond site.

[c7] 7. The method of claim 1, further comprising:
patterning the first conductive layer to remove conductive material adjacent to the bond site; and
applying bond pad material to the bond site after patterning the first conductive layer.

[c8] 8. The method of claim 1, further comprising:
applying an at least generally permanent protective coating over the first conductive layer;
preventing the protective coating from covering the bond site, or removing the protective coating from the bond site; and
applying bond pad material to the bond site after applying the protective coating.

[c9] 9. The method of claim 1, further comprising:
applying a soldermask coating over the first conductive layer;
removing the soldermask coating from the bond site;
treating the soldermask material to inhibit its removal from regions adjacent to the bond site; and
applying bond pad material to the bond site after applying the soldermask coating.

[c10] 10. The method of claim 1 wherein the bond site includes a first bond site, and wherein the method further comprises disposing bond pad material at a second bond site of the second conductive layer.

[c11] 11. The method of claim 1 wherein disposing bond pad material includes disposing at least one of nickel and gold.

[c12] 12. The method of claim 1 wherein disposing bond pad material includes disposing the bond pad material to wrap around an exposed edge of the first conductive layer at the bond site.

[c13] 13. The method of claim 1, further comprising:
attaching the support substrate to a microfeature die; and
electrically coupling the microfeature die to the bond pad of the support substrate.

[c14] 14. The method of claim 1 wherein exposing a support substrate to an electrolyte includes exposing a printed circuit board to the electrolyte.

[c15] 15. The method of claim 1 wherein exposing a support substrate to an electrolyte includes exposing a support substrate that is configured to carry a microelectronic die having semiconductor features, but that by itself does not include semiconductor features.

[c16] 16. A method for forming a support substrate for carrying microfeature dies, comprising:

exposing a support substrate to an electrolyte, the support substrate having a first side with a first conductive layer, a second side opposite the first side with a second conductive layer, and a conductive path extending

through the support substrate from the first conductive layer to the second conductive layer; and
forming bond pads at a first bond site of the first conductive layer and at a second bond site of the second conductive layer by disposing at least one conductive bond pad material at the bond sites, wherein disposing the at least one conductive bond pad material includes applying an electrical potential to the second conductive layer and passing an electrical current between the first conductive layer and the second conductive layer via the conductive path while the support substrate is exposed to the electrolyte.

[c17] 17. The method of claim 16 wherein the first bond pad site is one of multiple first bond pad sites, and wherein the second bond pad site is one of multiple second bond pad sites, and wherein forming the bond pads includes forming the first bond pads to have a first pitch and forming the second bond pads to have a second pitch coarser than the first pitch.

[c18] 18. The method of claim 16, further comprising
applying an at least generally permanent protective coating over the first conductive layer;
preventing the protective coating from covering the first bond site, or removing the protective coating from the first bond site; and wherein
disposing bond pad material at the bond pad sites includes disposing the bond pad material after applying the protective coating.

[c19] 19. The method of claim 16, further comprising:
(a) placing a removable protective coating over the second conductive layer;
(b) preventing the removable protective coating from covering the second bond site, or removing the protective coating from the second bond site;

- (c) applying conductive material to the first and second bond sites simultaneously, after performing processes (a) and (b);
- (d) removing the removable protective coating from the second conductive layer; and
- (e) patterning the second conductive layer by removing a portion of the second conductive layer while leaving the second bond site electrically coupled to the first bond site via the conductive path.

[c20] 20. The method of claim 19, further comprising:

- (f) applying an at least generally permanent protective coating over the first conductive layer;
- (g) preventing the protective coating from covering the first bond pad site, or removing the protective coating from the bond site; and wherein applying conductive material is performed after performing processes (a), (b), (f) and (g).

[c21] 21. The method of claim 16, further comprising:

- (a) placing a removable protective dry film coating over the second conductive layer;
- (b) preventing the removable protective dry film coating from covering the second bond site, or removing the protective dry film coating from the second bond site;
- (c) applying conductive material to the first and second bond sites simultaneously, after performing processes (a) and (b);
- (d) removing the removable protective dry film coating from the second conductive layer; and
- (e) patterning the second conductive layer by removing a portion of the second conductive layer while leaving the second bond site electrically coupled to the first bond site via the conductive path.

[c22] 22. The method of claim 16, further comprising:
attaching a microfeature die to the support substrate;
electrically connecting the microfeature die to the first bond site; and
applying a solder ball to the second bond site.

[c23] 23. A method for forming a support substrate for carrying microfeature dies,
comprising:

 patterning a first conductive layer on a first surface of a support substrate to
 form a bond site at the first surface, wherein the support substrate has
 a second surface facing opposite from the first surface, the second
 surface having a second conductive layer, and wherein the support
 substrate further includes a conductive path extending through the
 support substrate from the first conductive layer to the second
 conductive layer; and

 after patterning the first conductive layer, forming a bond pad at a bond site of
 the first conductive layer by passing an electrical current through the
 first and second conductive layers via the conductive path while the
 support substrate is exposed to an electrolyte.

[c24] 24. The method of claim 23 wherein passing an electrical current includes
passing an electrical current while the second conductive layer covers at least
approximately the entire second side.

[c25] 25. The method of claim 23 wherein passing an electrical current includes
passing an electrical current prior to patterning the second conductive layer to form bond
pads at the second conductive layer.

[c26] 26. The method of claim 23, further comprising:
applying an at least generally permanent protective coating over the first
conductive layer;

preventing the protective coating from covering the bond site, or removing the protective coating from the bond site; and
applying bond pad material to the bond site after applying the protective coating.

[c27] 27. The method of claim 23 wherein the bond site includes a first bond site, and wherein the method further comprises disposing bond pad material at a second bond site of the second conductive layer.

[c28] 28. The method of claim 23, further comprising:
attaching the support substrate to a microfeature die; and
electrically coupling the microfeature die to the bond pad of the support substrate.

[c29] 29. The method of claim 23 wherein exposing a support substrate to an electrolyte includes exposing a support substrate that is configured to carry a microelectronic die having semiconductor features, but that by itself does not include semiconductor features.

[c30] 30. The method of claim 23 wherein the bond site is a first bond site and wherein the method further comprises:

- (a) placing a removable protective dry film coating over the second conductive layer;
- (b) preventing the removable protective dry film coating from covering a second bond pad site at the second conductive layer, or removing the protective dry film coating from the second bond site;
- (c) applying a generally permanent protective coating to the first conductive layer and exposing or leaving exposed the first bond site
- (d) applying conductive material to the first and second bond sites simultaneously, after performing processes (a), (b) and (c)

- (e) removing the removable protective dry film coating from the second conductive layer;
- (f) patterning the second conductive layer by removing a portion of the second conductive layer while leaving the second bond site electrically coupled to the first bond site via the conductive path; and
- (g) applying a generally permanent protective coating over the second conductive layer after patterning the second conductive layer.

[c31] 31. A method for forming a support substrate for carrying microfeature dies, comprising:

applying an at least generally permanent protective coating over a first conductive layer of a support substrate, wherein the first conductive layer is positioned at a first surface of the support substrate and includes a first bond site, and wherein the support substrate further includes a second surface facing opposite from the first surface, the second surface having a second conductive layer with a second bond site;

preventing the protective coating from covering the first bond site, or removing the protective coating from the first bond site; and

applying bond pad material to the first and second bond pad sites after applying the protective coating.

[c32] 32. The method of claim 31 wherein removing the protective coating includes removing the protective coating prior to making it at least generally permanent, and wherein the method further comprises making the coating at least generally permanent by applying energy to the protective coating prior to applying bond pad material to the first and second bond sites.

[c33] 33. The method of claim xx wherein applying bond pad material includes applying an electrical potential to the second conductive layer and passing the electrical

between the first and second conductive layers via a conductive path extending through the support substrate while the support substrate is exposed to the electrolyte.

[c34] 34. The method of claim 33 wherein applying an electrical potential includes applying an electrical potential directly to the second conductive layer without applying the electrical potential directly to the first conductive layer, other than through the conductive path.

[c35] 35. A method for forming a support substrate for carrying microfeature dies, comprising:

- patterning a first conductive layer on a first surface of a support substrate to form a bond site at the first surface, wherein the support substrate has a second surface facing opposite from the first surface, the second surface having a second conductive layer, and wherein the support substrate further includes a conductive path extending through the support substrate from the first conductive layer to the second conductive layer;

- applying an at least generally permanent protective coating over the first conductive layer after patterning the first conductive layer;

- preventing the protective coating from covering the bond site, or removing the protective coating from the bond site; and

- applying bond pad material to the bond site after applying the protective coating, wherein applying bond pad material includes:

- exposing the support substrate to an electrolyte; and

- applying an electrical potential to the second conductive layer and passing an electrical current between the first and second conductive layers via the conductive path while the support substrate is exposed to an electrolyte.

[c36] 36. The method of claim 35 wherein the bond site includes a first bond site, and wherein the method further comprises:

patterning the second conductive layer to form a second bond site, wherein the second bond site is electrically coupled to the first bond site via the conductive path; and
applying conductive bond pad material to the second bond site.

[c37] 37. The method of claim 35 wherein the bond site includes a first bond site, and wherein the method further comprises:

placing a removable protective coating over the second conductive layer;
preventing the removable protective coating from covering a second bond site at the second conductive layer, or removing the removable protective coating from the second bond site;
applying conductive bond pad material to the second bond site simultaneously with applying conductive bond pad material to the first bond site;
removing the removable protective coating from the second conductive layer;
and
patterning the second conductive layer by removing a portion of the second conductive layer while leaving the second bond site electrically coupled to the first bond site via the conductive path.

[c38] 38. The method of claim 35 wherein the bond site includes a first bond site, and wherein the method further comprises:

placing a removable protective dry film coating over the second conductive layer;
preventing the removable protective dry film coating from covering a second bond site at the second conductive layer, or removing the removable protective dry film coating from the second bond site;
applying conductive bond pad material to the second bond site simultaneously with applying conductive bond pad material to the first bond site;

removing the removable protective dry film coating from the second conductive layer; and

patterning the second conductive layer by removing a portion of the second conductive layer while leaving the second bond site electrically coupled to the first bond site via the conductive path.

[c39] 39. The method of claim 35 wherein the bond site includes a first bond site, wherein the generally permanent protective coating includes a first generally permanent protective coating, and wherein the method further comprises:

- placing a removable protective coating over the second conductive layer;
- preventing the removable protective coating from covering a second bond site at the second conductive layer, or removing the removable protective coating from the second bond site;
- applying conductive bond pad material to the second bond site simultaneously with applying conductive bond pad material to the first bond site;
- removing the removable protective coating from the second conductive layer;
- patterning the second conductive layer by removing a portion of the second conductive layer while leaving the second bond site electrically coupled to the first bond site via the conductive path;
- applying a second at least generally permanent protective coating over the second conductive layer after patterning the second conductive layer;
- and
- preventing the second at least generally permanent protective coating from covering the second bond site, or removing the protective coating from the second bond site.

[c40] 40. The method of claim 35, further comprising keeping the at least generally permanent protective coatings in place after a microfeature die is attached to the support substrate.

[c41] 41. The method of claim 35 wherein applying an electrical potential to the second conductive layer and passing the electrical current between the first and second conductive layers includes applying the electrical potential and passing the electrical current through copper conductive layers.

[c42] 42. The method of claim 35 wherein applying the removable second protective coating includes applying a dry film.

[c43] 43. A microelectronic system, comprising:
a support substrate configured to carry a microfeature die, the support substrate having a first surface with a first conductive layer having multiple first bond sites, and a second surface facing opposite from the first surface, the second surface having a second conductive layer with multiple second bond sites;
conductive bond pad material positioned at the first bond sites to form first bond pads, the first bond pads being separated from each other by a first average spacing, the bond pad material extending around an edge of the first conductive layer at the first bond sites;
conductive bond pad material positioned at the second bond sites to form second bond pads, the first and second bond pads being electrically coupled with conductive pathways extending through the support substrate, the second bond pads being separated from each other by a second average spacing greater than the first average spacing, the bond pad material having a different arrangement at the second bond sites than at the first bond sites.

[c44] 44. The system of claim 43 wherein the bond pad material at the second bond sites is spaced apart from an edge of the second conductive layer at the second bond sites.

[c45] 45. The system of claim 43, further comprising conductive couplers attached to the second bond pad sites.

[c46] 46. The system of claim 43, further comprising:
a microfeature die carried by the support substrate and electrically coupled to the first bond pads of the support substrate; and
an external device electrically coupled to the second bond pads of the support substrate.

[c47] 47. The system of claim 43, further comprising a microfeature die carried by the support substrate and electrically coupled to the first bond pads of the support substrate.

[c48] 48. A microelectronic system, comprising:
a support substrate configured to carry a microfeature die, the support substrate having a first surface with a first conductive layer having multiple first bond sites, and a second surface facing opposite from the first surface, the second surface having a second conductive layer with multiple second bond sites;
conductive bond pad material positioned at the first bond pad sites to form first bond pads, the first bond pads being separated from each other by a first average spacing, the bond pad material extending around an edge of the first conductive layer at the first bond sites;
conductive bond pad material positioned at the second bond pad sites to form second bond pads, the first and second bond pads being electrically coupled with conductive pathways extending through the support substrate, the second bond pads being separated from each other by a

second average spacing greater than the first average spacing, the bond pad material being offset laterally from an edge of the of the second conductive layer at the second bond sites;
a first at least generally permanent protective coating positioned adjacent to the first bond pads; and
a second at least generally permanent protective coating positioned on the second surface.

[c49] 49. The system of claim 48, further comprising conductive couplers attached to the second bond pad sites.

[c50] 50. The system of claim 48, further comprising:
a microfeature die carried by the support substrate and electrically coupled to the first bond pads of the support substrate; and
an external device electrically coupled to the second bond pads of the support substrate.

[c51] 51. The system of claim 48, further comprising a microfeature die carried by the support substrate and electrically coupled to the first bond pads of the support substrate.