

PATENT SPECIFICATION

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(54) ELECTRONIC TIME INDICATING STRUCTURE

(71) We, KABUSHIKI KAISHA SUWA SEIKOSHA, a Japanese company, of 3—4, 4-chome, Ginza, Chuo-ku, Tokyo, Japan, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to electronic time indicating structures and, in particular, although not so restricted, to time indicating structures for electronic watches.

In conventional electronic watches correction of the time indication can only be effected with difficulty and so, in this respect at least, electronic watches are inferior to mechanical watches. In fact, some electronic watches fail to provide any mechanism whereby time correction can be effected and merely include means whereby the time indication can be zeroed.

The present invention seeks to avoid these disadvantages of known time indicating structures.

According to one aspect of the present invention there is provided an electronic time indicating structure comprising an oscillator for producing a relatively high frequency electrical signal, a frequency divider for producing from said relatively high frequency signal a relatively low frequency signal, timing signal means for producing from said relatively low frequency signal a plurality of different frequency timing signals, an indicating device for each timing signal for providing a visual time indication thereof, first switch means for substantially simultaneously changing the time indication of all the indicating devices, and second switch means for selectively resetting the time indication of each of said indicating devices.

Said oscillator may be a crystal oscillator.

Each indicating device may be a liquid crystal display means.

Preferably each timing signal means comprises a counter means having an input and an output arranged so that, in operation, the

output frequency is $1/n$ the input frequency where n is a whole number.

The frequency divider preferably includes complementary-symmetry metal oxide semiconductor devices.

The time indicating structure may include at least timing means for producing a timing signal corresponding to minute intervals, timing means for producing a timing signal corresponding to 10-minute intervals and timing means for producing a timing signal corresponding to hour intervals. Furthermore, the time indicating structure may include timing means for providing a timing signal corresponding to 1-second intervals and timing means for providing a timing signal corresponding to 10-second intervals.

The frequency divider preferably is arranged to provide a low frequency signal of 1 Hz.

According to a further aspect of the present invention, there is provided a timepiece or an electronic watch having such an electronic time indicating structure.

The invention is illustrated, merely by way of example, in the accompanying drawings, in which:

Figure 1 is a block diagram of an electronic watch according to the present invention;

Figure 2 illustrates an inverter with use of the electronic watch of Figure 1; and

Figure 3 is a circuit diagram of one-stage of a frequency divider for the electronic watch of Figure 1.

Referring first to Figure 1 there is shown a block diagram of an electronic watch according to the present invention. The electronic watch comprises a crystal oscillator X which generates a relatively high frequency output signal, the frequency of which may be 2^n Hz, where n is a whole number. A time indication is produced by counting cycles of the output signal from the oscillator.

The output signal from the oscillator X is amplified in an amplifier 11, the output of which is fed to a first inverter 12, one half

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the output signal of which is fed directly to a ripple carry counter or frequency divider block 1 and the other half of the signal of which is fed to a second inverter 13. The output signal from the second inverter is also fed to the block 1. Thus the block 1 receives two input signals of a frequency 2^n Hz and out of phase by 180° .

The block 1 has a plurality of stages, for example, it may have n stages so the output therefrom at an output terminal Q is 1 Hz. One of the stages of the block 1 is illustrated in Figure 3 which, it is thought, will be found largely self-explanatory. If the stage illustrated in Figure 3 is the first stage of the

block 1 the inputs ϕ and $\bar{\phi}$ will correspond to the outputs of the inverters 12, 13 respectively which outputs are shown graphically in Figure 3. The output from this stage is

shown by Q and $\bar{Q}$ which are 180° out of phase and half the frequency of the inputs ϕ

and $\bar{\phi}$ to this stage. A re-set signal may be applied to block 1 at the terminal R. As illustrated graphically in Figure 3 when this re-set signal is high, i.e. at a voltage V_{DD} , then the voltage is applied to all stages of the block 1 so that the dividing operation ceases and the output from each stage and from the block 1 as a whole is a non-alternating voltage. That is to say, when the re-set signal is applied to the frequency divider the output thereof is zeroed. When the re-set signal is low, i.e. at a voltage V_{SS} , the block 1 is in its normal operating condition and its output frequency may be 1 Hz.

The block 1 shown in Figure 3 is comprised of complementary-symmetry type metal oxide semiconductors referred to hereinafter as COS/MOS.

The output of the block 1 is fed via a capacitor C1 to a first inverter 14 one half of the output signal of which is fed directly to a decade counter and decoder block 2 and the other half of which is fed to a second inverter 15. The output signal from the second inverter 15 is also fed to the block 2. Thus the input signals to the block 2 comprise two 1 Hz frequency signals 180° out of phase. The output signal of the block 2 at an output terminal Q is 10-second signal (i.e. an output signal of a frequency of $1/10$ th Hz.). At the same time the block 2 rectifies the 1 Hz frequency signal output and applies the same via a line 16 to drive a units second indication 17 of a digital display panel 7.

The 10-second signal from the block 2 is fed to a $1/6$ th counter and decoder block 3 via a capacitor and two inverters arranged in similar manner to the capacitor C1 and the inverters 14, 15. The input signals to the block 3 comprise two 10-second signals 180°

out of phase. The output signal of the block 3 at an output terminal Q is a minute signal (i.e. an output signal of a frequency of $1/60$ th Hz). The 10-second signal is rectified in the block 3 and applied to a 10-seconds indication 18 of the panel 7 via a line 19.

The minute signal from block 3 is fed to a decade counter and decoder block 4 via a capacitor and two inverters arranged in similar manner to the capacitor C1 and the inverters 14, 15. The input signals to the block 4 comprise two $1/60$ th Hz signals 180° out of phase. The output signal of the block 4 at an output terminal Q is a 10-minute signal, (i.e. an output signal of a frequency of $1/600$ th Hz). The 1-minute signal is rectified in the block 4 and applied to a units minute indication 20 of the panel 7 via a line 20.

The 10-minute signal from the block 4 is fed to a $1/6$ th counter and decoder block 5 via a capacitor and two inverters again arranged in similar manner to the capacitor C1 and the inverters 14, 15. The input signals to the block 5 comprise two $1/600$ th Hz signals 180° out of phase. The output signal of the block 5 at an output terminal Q comprises a 1-hour signal, (i.e. an output signal of a frequency of $1/3600$ th Hz). The 10-minute signal is rectified in the block 5 and applied to a 10-minutes indication 22 via a line 23.

Finally, the 1-hour signal from the block 5 is fed to a $1/24$ th frequency counter and decoder block 6 via a capacitor and two inverters arranged in similar manner to the capacitor C1 and the inverters 14, 15. The input signals to the block 6 comprise two $1/3600$ th Hz frequency signals 180° out of phase. The 1-hour signal is rectified in the block 6 and is applied to an hours indication 24 via a line 25.

A re-set signal can be applied to a respective terminal R of each of blocks 1 to 6 by closing a switch S1 so that a voltage V_{DD} is applied to each terminal R from a rail 28. Thus by closing the switch S1 all the blocks are re-set so that the panel 7 is zeroed, i.e. indicates zero hours, zero minutes, and zero seconds. By making the switch S1 an ON-OFF switch the electronic watch may be used as a stopwatch.

In the case of an ordinary watch, merely to provide a switch S1 for the purpose of correcting the time indication would be highly inconvenient because this could only be accomplished at midnight every twenty four hours.

Therefore, a second switch S2 is provided to enable the block 1 to be re-set on its own without affecting the other blocks. Similarly, switches S3 to S7 are provided to re-set blocks 2 to 6 respectively. The switches S3 to S7 are connected to a rail 29 which is at a

voltage V_{DD} by a line 30. Thus when the switch S2 is closed the voltage V_{DD} from the rail 29 is applied to the terminal R of the block 1 so that it is zeroed. The output from the block 1 is kept at a voltage V_{ss} by resistor R1 and the capacitor C1 which biases off the DC component of the output. When the switch S3 is closed the input to the inverter 14 is at a voltage V_{DD} . Thus when the switch S3 is closed and then re-opened, i.e. it is pulsed, a pulse is applied to the block 2 and the units second indication 17 increases its time indication by unity. By continued pulsing of the switch S3 any required units second time can be achieved. Similarly by pulsing switch S4 any required 10-seconds time indication can be achieved and so on with switch S5 to S7.

If the electronic watch only gives a time indication in minutes and hours the switch S2 can be arranged to re-set blocks 1, 2, 3 simultaneously the correction of the time indication being effected by switches S5 to S7. Thus a time correction can be effected once every minute.

Each of the inverters may be of the COS/MOS type as illustrated in Figure 2 which also shows the input and output waveforms of such an inverter.

The display panel 7 may include liquid crystal display means.

It will be appreciated with the above described electronic watch that the switch S1 causes all the blocks 1 to 6 to be zeroed substantially simultaneously and the switches S2 to S7 enable the time correction resulting from the blocks 1 to 6 to be re-set selectively. Therefore, in this electronic watch time correction may be performed easily without any special skill being required.

Attention is directed in pursuance of Section 9 of the Patents Act 1949 to our Patent No. 1,285,012.

WHAT WE CLAIM IS:—

1. An electronic time indicating structure comprising an oscillator for producing a relatively high frequency electrical signal, a frequency divider for producing from said relatively high frequency signal a relatively low frequency signal, timing signal means for producing from said relatively low frequency signal a plurality of different frequency timing signals, an indicating device for each timing signal for providing a visual time indication thereof, first switch means for substantially simultaneously changing the time indication of all the indicating devices, and second switch means for selectively resetting the time indication of each of said indicating devices.

2. A structure as claimed in claim 1 in which said oscillator is a crystal oscillator.

3. A structure as claimed in claim 1 or 2 in which each indicating device is a liquid crystal display means.

4. A structure as claimed in any preceding claim in which each timing signal means comprises a counter means having an input and an output arranged so that, in operation, the output frequency is $1/n$ the input frequency where n is a whole number.

5. A structure as claimed in any preceding claim in which the frequency divider includes complementary-symmetry metal oxide semiconductor devices.

6. A structure as claimed in any preceding claim including at least timing means for producing a timing signal corresponding to minute intervals, timing means for producing a timing signal corresponding to 10-minute intervals and timing means for producing a timing signal corresponding to hour intervals.

7. A structure as claimed in claim 6 further including timing means for providing a timing signal corresponding to 1-second intervals and timing means for providing a timing signal corresponding to 10-second intervals.

8. A structure as claimed in claim 7 in which the frequency divider is so arranged to provide a low frequency signal of 1 Hz.

9. An electronic time indicating structure substantially as herein described with reference to and as shown in the accompanying drawings.

10. An electronic time indicating structure comprising a crystal oscillator for producing a relatively high frequency electrical signal, a frequency divider composed of COS/MOS semi-conductor devices for producing from said relatively high frequency signal a relatively low frequency signal, a digital indicating device for each timing signal for providing a visual time indication thereof, switch means for selectively changing the time indication of each said indicating device, each operation of the switch means changing the time indication of the respective indicating device by one digit.

11. A timepiece having a time indicating structure as claimed in any preceding claim.

12. An electronic watch having a time indicating structure as claimed in any of claims 1 to 10.

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voltage V_{DD} by a line 30. Thus when the switch S2 is closed the voltage V_{DD} from the rail 29 is applied to the terminal R of the block 1 so that it is zeroed. The output from the block 1 is kept at a voltage V_{ss} by resistor R1 and the capacitor C1 which biases off the DC component of the output. When the switch S3 is closed the input to the inverter 14 is at a voltage V_{DD} . Thus when the switch S3 is closed and then re-opened, i.e. it is pulsed, a pulse is applied to the block 2 and the units second indication 17 increases its time indication by unity. By continued pulsing of the switch S3 any required units second time can be achieved. Similarly by pulsing switch S4 any required 10-seconds time indication can be achieved and so on with switch S5 to S7.

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9. An electronic time indicating structure substantially as herein described with reference to and as shown in the accompanying drawings.

10. An electronic time indicating structure comprising a crystal oscillator for producing a relatively high frequency electrical signal, a frequency divider composed of COS/MOS semiconductor devices for producing from said relatively high frequency signal a relatively low frequency signal, a digital indicating device for each timing signal for providing a visual time indication thereof, switch means for selectively changing the time indication of each said indicating device, each operation of the switch means changing the time indication of the respective indicating device by one digit.

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