

RADIO TRANSMITTING AND RECEIVING CIRCUITS OF A
VIDEO CAMERA HAVING A DETACHED VIEW FINDER

The present invention relates to video cameras wherein a view finder
5 is detached from the main body, and more particularly to radio transmitting
and receiving circuits provided in a video camera operated with detached main
body and view finder sections.

Generally, a view finder of a video camera (or a camcorder) is
10 integrated with the main body of the video camera and is operated and
supported within a common housing. An alternative is the detached video
camera disclosed in U.S. Patent No. 4,541,698 by Lerner, where the view
finder is detached from the video camera's main body which is mounted
somewhere on the user's body, but connected via wires. However, since this
15 is not wireless, photographing in inconvenient places, e.g. under water or in
corners, is limited by such cramped spaces, rendering the video camera
inconvenient to use. In addition to this, U.S. Patent No. 4,672,436 by
Hawthorn discloses a radio transmitter/receiver in which a detached view
finder and the main body of a video camera can communicate with each other
20 by radio, but does not teach a technique for processing the video signal
without interference.

Preferred embodiments of the present invention aim to solve the above
problem and to provide in a video camera a radio transmitting circuit and a
25 radio receiving circuit provided in the main body and the view finder,
respectively, which are detached and operated by radio.

Another aim is to provide a radio transmitting circuit for transmitting a digital coding signal set by a user which is superposed on a video signal by applying a coding technique, and a radio receiving circuit for receiving a video signal only if the digital coding signal equals the value stored in the view finder, so as to prevent interference of the operating signals between video cameras operated by radio.

According to a first aspect of the present invention, there is provided a radio transmitting circuit which is installed in a main body of a video camera having a detached view finder, the circuit comprising:

a CCD portion for converting an image signal of an object input through a lens of said video camera into an electrical signal;

a preprocessor for receiving the electrical signal to perform an automatic white balance control, an automatic black balance control, a flare compensation, and a gamma compensation;

a video signal processor for receiving the preprocessed signal, performing a luminance/colour difference signal process, and outputting a composite video signal;

a synchronous signal separator for separating the composite video signal output from said video signal processor into vertical and horizontal synchronizing signals;

code means for encoding a code set through a keypad by a user to provide a code signal;

a timing controller for receiving the code signal output from said code means and overlapping the code signal on a predetermined horizontal synchronizing signal interval within the horizontal synchronizing signal separated in said synchronous signal separator;

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a mixer for mixing the overlapped signal of said timing controller and the video signal of said video signal processor;

a modulating portion for receiving the mixed signal from said mixer
10 and modulating the received mixed signal by a carrier of a specific frequency;
and

a transmitting portion for amplifying the modulated video signal of said modulator in an amplifier and then transmitting the amplified signal to said
15 view finder through a transmitting antenna by radio.

Preferably, said timing controller comprises:

a counter for receiving and counting a horizontal synchronizing signal
20 separated in said synchronous signal separator and outputting the result;

an A/D converter for receiving a clock signal from said counter to convert the analog vertical synchronizing signal detached in said synchronizing signal separator into a digital signal;

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a memory for storing the converted digital signal in an assigned address in response to an address signal from the counter;

a read/write control logic portion for supplying a read/write logic signal to the memory in response to the output from said counter to read/write the vertical synchronizing signal stored in the memory;

5 a D/A converter for converting the digital vertical synchronizing signal read and written in said memory according to the control signal of said read/write control logic portion, into an analog signal in response to a clock signal from said counter;

10 a monostable multivibrator for delaying by a predetermined width the analog-converted vertical synchronizing signal from said D/A converter;

a gate circuit for gating an output from said counter and the output from said multivibrator and passing only a predetermined horizontal synchronizing signal;

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an AND gate for receiving and AND-gating the inverted signal of the output of said gate circuit and said video signal and outputting the logic result; and

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an adder for adding a horizontal synchronizing signal output from said AND gate to the output signals of said encoder.

Preferably, said code means comprises;

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a code generator for generating a code using the digits 0 through 9 input through said keypad by a user; and

an encoder for encoding said code from said code generator to provide said code signals to be supplied to said timing controller.

According to another aspect of the present invention, there is provided
5 a radio receiving circuit of a video camera having a detached view finder in which said circuit is installed, said circuit comprising:

a receiving portion for receiving through a receiving antenna a signal transmitted by radio from a main body of said video camera, from which the
10 view finder is detached;

a demodulator for amplifying and detecting the received signal supplied from said receiving portion;

a video signal processor for processing the detected video signal
15 supplied from said demodulator;

a synchronous signal separator for separating said video signal into vertical and horizontal synchronizing signals;

20 a timing controller for extracting a code signal overlapped on a predetermined horizontal synchronizing signal interval separated in said synchronizing signal separator;

decoding means for comparing and discriminating the decoded signal
25 of the code signal supplied from said timing controller and a predetermined code set through a keypad by a user;

a gating portion for passing or stopping the video signal supplied from said video signal processor in response to the signal supplied from said decoding means; and

5 a display portion for receiving the video signal from said gating portion if passed thereby, amplifying the received video signal, separating a synchronizing signal, and then displaying a video signal on the screen of the view finder.

10 Preferably, said timing controller comprises:

a counter for receiving and counting the horizontal synchronizing signal separated in said synchronous signal separator and producing outputs;

15 an A/D converter for receiving a clock signal from said counter and converting an analog vertical synchronizing signal separated in said synchronous signal separator into a digital signal;

20 a memory for storing the digital-converted signal into an assigned address in response to an address signal from said counter;

a read/write control logic portion for supplying a read/write logic signal to said memory in response to the output from said counter to read/write the vertical synchronizing signal stored in said memory;

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a D/A converter for converting the digital vertical synchronizing signal read and written from said memory according to the control signal of said

read/write control logic portion into an analog signal in response to a clock signal from said counter;

5 a monostable multivibrator for delaying by a predetermined width the analog-converted vertical synchronizing signal from said D/A converter;

a gate circuit for gating an output from said counter and the output from said multivibrator and passing only a predetermined horizontal synchronizing signal; and

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an AND gate for receiving and AND-gating the inverted signal of the output of said gate circuit and said video signal and outputting the logic result.

Preferably, said decoding means comprises:

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a code generator for generating a code using the digits 0 through 9 input through said keypad by a user;

20 a decoder for decoding a cryptic code loaded on the horizontal synchronizing signal of the video signal output from said timing controller; and

a code discriminator for receiving the output from said code generator and the output from said decoder and comparing and discriminating whether the two output signals match or not, and transmitting a corresponding signal to said gating portion.

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The invention extends to a video camera provided with a transmitting and/or receiving circuit according to any of the preceding aspects of the invention.

5 According to a further aspect of the present invention, there is provided a video camera comprising a plurality of parts contained in separate housings; a radio transmitter associated with one of said parts for transmitting video information from said one part; a radio receiver associated with another of said parts for receiving video information transmitted from said transmitter;
10 and encoding means for setting first and second identifying codes for said transmitter and receiver respectively such that video information received by said receiver is fully processed only when said first code in a received signal has a predetermined relationship with said second code.

15 For a better understanding of the invention, and to show how the same may be carried into effect, reference will now be made, by way of example, to the accompanying diagrammatic drawings, in which:

20 Figure 1 is a block diagram showing the constitution of one example of a radio transmitting circuit adapted to a main body of a video camera according to the present invention;

Figure 2 is a block diagram showing the constitution of one example of a radio receiving circuit adapted to a remote, detached view finder of the video camera;

5 Figures 3A through 3E are waveform diagrams for explaining an example of an encoding operation of a radio transmitting circuit of Figure 1, and show waveform diagrams of part of a TV broadcasting signal, a separated vertical synchronizing signal, a delayed and waveform-transformed synchronizing signal used as a gate pulse, a separated horizontal synchronizing pulse, and an encoded horizontal synchronizing pulse, respectively;

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Figure 4A is a detailed block diagram of one example of the constitution of a timing controller of the circuit of Figure 1;

15 Figure 4B is a detailed block diagram of one example of a timing controller of the circuit of Figure 2;

Figure 5 is a detailed circuit diagram of one example of a code means of the circuit of Figure 1; and

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Figure 6 is a diagram showing the constitution of another example of an embodiment of the invention, in which a radio receiving circuit of a view finder is realized using a microcomputer.

25 Referring to Figure 1, light reflected from an object passes through a camera lens portion A of a video camera. At this time, the light entering camera lens portion A is controlled by an automatic focusing driver, an automatic iris driver, and a shutter (not shown) and then is converted into an

electrical video signal by a charge-coupled device (CCD) 10 which is an image pickup device. The converted output signal is processed in a preprocessor 20 by an automatic white balance control, an automatic black balance control, a flare compensation, and a gamma compensation, and
5 supplied to a video signal processor 30 to be separated into a luminance signal and a colour difference signal and output as a video signal which includes a composite synchronizing signal. The processed video signal is transmitted with the composite synchronizing signal directly to VCR deck B to be recorded or reproduced. At this time, an audio signal is also supplied to the
10 VCR deck B through a microphone (not shown) to be recorded. The aforementioned video signal processing techniques are generally well-known to those skilled in the art, and accordingly, a more detailed description thereof is not given here.

15 In the process which is now described in more detail, video signals are transmitted/received by wireless from the main body of a video camera to the screen of the view finder, which is detached from the main body.

The video signal supplied from the video signal processor 30 is
20 supplied to a synchronous signal separator 40 to be separated into vertical and horizontal synchronizing signals and then supplied to a timing controller 60. Meanwhile, within a code means 50, a user can input a secret number through numbered keys (0-9) and other function keys using a code generator 51 which includes a keypad. Accordingly, the code generator 51 generates a digital
25 signal corresponding to the entered secret number. The digital signal is input to an encoder 52 to be encoded (also within code means 50), and then is supplied to the timing controller 60. Encoder 52 is a 10-to-4 bit coder which encodes a decimal digit from code generator 51, converting it into 4-bit digital

data. the timing controller 60 overlaps the digital data signal supplied from the code means 50 on a horizontal synchronizing signal interval corresponding to 10H - 13H within the character signal insertion interval of the horizontal synchronizing signal separated in the synchronous signal separator 40 and if
5 each vertical synchronizing pulse is greater than a reference pulse, it acts as a high, and if it is lower than the reference pulse, it acts as a low. The overlapped signal from the timing controller 60 is supplied to a mixer 70 along with the signal directly from the video signal processor 30, i.e. the video signal in which the synchronizing signal has not been separated. These
10 two signals are mixed in mixer 70 and then supplied to a modulating portion 80. The mixed signal is modulated in modulator 82 by means of a carrier of a specific frequency of a carrier oscillator 81 within modulating portion 80. The modulator 82 uses a balanced modulator or some other type of amplitude modulator. The modulated video signal from modulator 80 is amplified
15 through an amplifier 91 and transmitted via a transmitter 92 and a transmitting antenna 93, which together constitute a transmitting portion 90, and ultimately received by the view finder by way of a wireless link.

Referring to Figure 2, the signal radiated by wireless from the
20 transmitting portion 90 of the radio transmitting circuit, which is adapted to (e.g. housed in) the main body of the video camera, is received in a receiving portion 100 which is adapted to (e.g. housed in) the view finder of the video camera, and which is composed of a receiving antenna 101 and a receiver 102. The received signal is supplied to a demodulator 110 in which the signal
25 is amplified through an amplifier 111 and is detected in a detector 112. The detected video signal from demodulator 110 is supplied to a video signal processor 120 and processed therein. Here, the particular demodulator used determines whether the detector type employed as detector 112 is a

synchronous or nonsynchronous detector. This composite video signal processed in the video signal processor 120 is supplied to a synchronous signal separator 130 to be separated into vertical and horizontal synchronizing signals which are input to a timing controller 140 together with the composite video signal.

The timing controller 140 extracts the 4-bit digital signal loaded on the 10H - 13H interval of the horizontal synchronizing signal which is within the character signal insertion interval of the first field in the horizontal synchronizing signal, and then supplies the extracted digital signal to a decoding means 150. Meanwhile, the timing controller 140 extracts the 4-bit digital signal loaded on the horizontal synchronizing signal and then supplies the extracted signal to the decoding means 150. The timing controller 140 extracts a 4-bit digital signal loaded on the 273H - 276H interval of the horizontal synchronizing signal of a second field. The extracted 4-bit digital signal is supplied to the decoder 152 within the decoding means 150 and then, in the code discriminator 153, is compared with and discriminated against the code generated from the code generator 151 which includes a keypad. As the result of being decoded and discriminated in the decoding means 150, when the code from the code generator 151 equals the signal from the decoder 152, a logic high is output to the gating portion 160, thereby enabling the video signal supplied from the video signal processor 120 to the gating portion 160 to be fed to a display portion 170 to be displayed. Here, display portion 170 consists of a video amplifier and synchronous signal separator 171 for receiving and amplifying the video signal supplied from gating portion 160 and separating the synchronizing signals, and an electronic view finder (EVF) 172. When the code from the code generator 151 does not match the signal from the decoder 152, a low logic signal is input to the gating portion 160 to

cut-off the video signal supplied from the video signal processor 120, so that the image is not displayed in the electronic view finder 172.

Hereinafter, an example of operations of the radio transmitting and receiving circuits of the video camera having a detached view finder and constituted as above, will be described.

Figures 3A, 3B, 3C, 3D and 3E show waveform diagrams of a signal illustrating part of a TV broadcasting signal, a separated vertical synchronizing signal, a delayed and waveform-converted synchronizing signal as a gate pulse, a detached horizontal synchronizing pulse, and an encoded horizontal synchronizing pulse, respectively. These waveform diagrams serve to explain the encoding operation of the radio transmitting circuit of the video camera with separated view finder.

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First of all, this embodiment of the present invention uses a part of the horizontal synchronizing signal interval detached in the synchronous signal separator 40 of Figure 1. Referring to Figure 3A, the TV broadcasting signal has 525 scanning lines per scanned frame, while being divided into two fields for each frame. At the beginning, equalizing pulses T1 and T3 correspond to the 1H - 3H and the 7H - 9H intervals of the first field, respectively. The 4H - 6H interval T2 corresponds to the vertical synchronizing pulse. Also, the 10H - 20H interval T5 is where a multiple character data signal can be inserted. The interval where the character signal is inserted in the following second field is from 273H - 283H. Thus, as shown in Figure 3A, the vertical blanking interval of the signal with respect to one field of a TV broadcasting signal, consists of a 3H equalizing pulse interval T1, a 3H vertical synchronizing signal pulse interval T2, another 3H equalizing pulse interval

T3, a 10H - 20H character signal insertion interval T5, and other video signal intervals. As for the timing of the second field, the vertical blanking starting point is delayed by 0.5H with respect to the first field. That is, it starts at 263H.

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The timing controller 60 of the radio transmitting circuit shown in Figure 1 uses the 10H - 13H interval T4 within character signal insertion interval T5 to overlap the signal encoded through code means 50. Concurrently, timing controller 140 of the radio receiving circuit shown in Figure 2 extracts and decodes the data loaded in that interval T4, and checks whether it equals the preset code in the decoding means 150 of Figure 2. This is the function which prevents radio interference by discriminating a cryptic number. The picture is displayed on EVF 172 only if the codes match.

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The vertical and horizontal synchronizing signals separated in the synchronous signal separator 40 are supplied to the timing controller 60 (Figure 1). As shown in Figures 3B and 3C, the timing controller 60 delays the vertical synchronizing signal by 6H and produces a gate pulse signal whose pulse width is increased from 3H to 4H, thereby extracting only the 10H - 13H portion of the video signal input to the timing controller 60.

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A key signal is generated from the code generator 51 which includes a keypad and is input to encoder 52. Encoder 52 is a 10-to-4 bit coder in which the entered code becomes a parallel 4-bit digital signal to be supplied to the timing controller 60. According to the 4-bit digital signal composed of "1" and "0's" input to timing controller 60, the 10H - 13H pulse width of the horizontal synchronizing signal extracted in 1H unit from the least significant

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bit (LSB) to the most significant bit (MSB) is either incremented or maintained. Here, as shown in Figures 3D and 3E, when the 4-bit digital signal is "1", the pulse width of 10H - 13H horizontal synchronizing signal is increased in amplitude, and when it is "0", a converting step is carried out while retaining the original value, and then a pulse amplitude modulated (PAM) signal is output. As shown in Figure 1, after the PAM signal is mixed with the video signal in the mixer 70, it is modulated in the balanced modulating portion 80 or AM modulating portion and is amplified through the transmitting portion 90 to be transmitted from the transmitting antenna 93 to the view finder.

On the view finder side (Figure 2), receiving portion 100 receives the transmitted radio wave from the main body of the video camera through receiving antenna 101. The receiving portion uses a fixed receiving tuner tuned to a predetermined frequency. After the received signal is amplified and detected through demodulator 110 and processed in video signal processor 120, synchronous signal separator 130 separates the vertical and horizontal synchronizing signals from the composite video signal just as does the transmitting circuit. Then, both synchronizing signals and the video signal are all input to the timing controller 140. Like the timing controller 60 in the radio transmitting circuit in the main body of the video camera, timing controller 140 delays the vertical synchronizing signal by 6H and produces a gate pulse whose width is increased to 4H, thereby extracting the 10H - 13H interval of the horizontal synchronizing signal from the horizontal synchronizing signal input to the timing controller 140. This extracted signal is supplied to the decoder 152 of decoding means 150.

Decoder 152 sets a midpoint voltage between the levels of the logic "1's" and the logic "0's" in the 10H - 13H interval T4 as a detection reference voltage, then detects the logic levels encoded onto interval T4. At this time, if the level of the horizontal synchronizing signal is greater than the set reference voltage, a logic "1" is detected, and if it is lower, a "0" is detected. The detected data signal is converted back into a 10-bit digital signal in the same order, i.e. from LSB to MSB, as was encoded in the transmitting circuit of the video camera's main body to be supplied to code discriminator 153. Meanwhile, if an identical code is entered into the code generator 151 of decoding means 150 (which also includes a keypad), a 10-bit digital signal is input to the code discriminator 153. Discriminator 153 determines whether the user's entered code signal equals the code signal loaded on the input video signal. If the two coded signals match, an identification signal in the form of a logic high is supplied to the gating portion 160. The gating portion 160 thus enabled supplies a video signal to the EVF 172, thereby displaying a picture. Conversely, if the signals are not equal, the gating portion 160 cuts off the video signal, thereby automatically preventing interference with video signal input from other radio video cameras.

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Next, examples of the internal constitution of the timing controllers of the transmitting and receiving circuits of Figures 1 and 2 will be described. Figures 4A and 4B are detailed block diagrams of examples of the constitutions of the timing controllers 60, 140 shown in Figures 1 and 2, respectively.

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Referring to Figure 4A, the vertical synchronizing signal 141 and the horizontal synchronizing signal 142 separated in the synchronous signal

separator 40 are input to an A/D converter 143 and a counter 144, respectively. At this time, the horizontal synchronizing signal includes an equalizing pulse, and two equalizing pulses are input as a horizontal synchronizing signal to the counter 144 to be counted. An output of the counter 144 provides a clock signal CLK to the A/D converter 143, thereby sampling the vertical synchronizing signal input to the A/D converter 143 to be converted into a digital signal. The digital signal is output to a memory 145 and stored in an address of memory 145 assigned by address signal ADDR from counter 144. Meanwhile, another output of the counter 144 is supplied to a read/write control logic portion 146 to write the signal in the 1H - 6H interval and read from the 7H interval. The output of the read/write control logic portion 146 is supplied to memory 145 and reads the vertical synchronizing data written by the write signal in response to the read signal to be supplied to a D/A converter 147. In this case, a high logic signal can be directly output from counter 144 to memory 145 in the 1H to 6H interval, and a low logic signal can be directly output after the 7H interval.

Next, the vertical synchronizing signal input to the D/A converter 147 receives the clock signal CLK from counter 144, to be converted into an analog signal. The converted vertical synchronizing signal is stretched to a 4H width by a monostable multivibrator (M/M) 148 to be supplied to one terminal of the gating circuit 149. The gating circuit 149 generates a gate pulse of the waveform shown in Figure 3C. The gate pulse is inverted in an inverter 250 to be supplied to an AND gate 251. The AND gate 251 receives the output signal of the inverter 250 and the video signal and outputs the 10H - 13H video signal of the horizontal synchronizing signal as shown in Figure 3D. The 10H - 13H video signal is added to the output of code means 50 in

an adder 252, thereby supplying mixer 70 with a video signal loaded with coded information having the waveform shown in Figure 3E.

Referring to Figure 4B, the constitution and function of timing controller 140 adapted to the radio receiving circuit are very similar to those of timing controller 60 adapted in the radio transmitting circuit. In Figure 4B, references with a prime denote parts corresponding to those with the same reference (unprimed) in Figure 4A. A detailed description thereof will therefore not be repeated. In timing controller 140 of the radio receiving circuit, the output of AND gate 251' is directly supplied to decoding means 150, and accordingly the 10H - 13H interval horizontal synchronizing signal on which the cryptic code is loaded is discriminated with a reference code signal. The result of this discrimination is supplied to gating portion 160 of Figure 2 and gates the video signal.

Figure 5 shows an example of a detailed construction of the code means 50 of Figure 1, which comprises the code generator 51 and the encoder 52.

Referring to Figure 5, the user's key signal from the keypad of the code generator 51 in the transmitting circuit within the main body of the video camera, is a 10-bit digital signal and is converted into 4 bits by encoder 52 which includes a logic circuit. The respective converted digits are synchronized to the 10H to 13H pulses of the horizontal synchronizing signal to individually pass through respective AND gates. If a logic high results, a DC voltage is output by a DC bias circuit to be added to the 10H - 13H pulses of the horizontal synchronizing signal in respective adders and to be supplied to timing controller 60. In the timing controller 60, a code signal

from code means 50 is loaded onto the 10H - 13H interval of the horizontal synchronizing signal of the video signal.

5 Since the constitution and operation of decoder 152 and code generator 151 included in decoding means 150 of the radio receiving circuit of the view finder is very similar to that of code means 50 of the above radio transmitting circuit, its analogous operation will readily be understood by those skilled in the art, and therefore a detailed description will not be repeated.

10 The functions of the code generator, the decoder, the encoder, the code discriminator and the timing controller adapted to the radio transmitting and receiving circuits can be duplicated by software installed in a microcomputer 2 - for example, as shown in Figure 6, which illustrates in outline the constitution of a radio transmitting circuit using microcomputer 2.

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Referring to Figure 6, microcomputer 2 adds an encoding signal P2 to the 10H - 13H interval of the horizontal synchronizing signal according to a key input from a keyboard 1 and uses the vertical synchronizing signal as a gate pulse P1 synchronized to the horizontal synchronizing signal. The vertical synchronizing signal is then gated with a TV video signal through a gating device 4. In an adder 5, the gated signal is added to the horizontal synchronizing signal which carries the encoding signal, then is modulated through a modulator 6 and an amplifier 7 in a modulating portion 9 to be transmitted through a transmitting antenna 8. The above brief description
20 omits a detailed discussion of the constitution and flowchart of the microcomputer 2, but examples of these will readily be apparent to those skilled in the art, especially in the light of the foregoing description, and the scope of the present invention generally includes the same.

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In the above-described embodiments of the present invention, the radio transmitting and receiving circuits facilitate use of the video camera having a detached view finder in places where photographing is difficult or where space is limited. The possibility of interference from a video signal from another radio video camera is reduced, by use of a cryptic code which can readily be set by the user through a keypad.

Although the above-described embodiments of the invention provide a radio link between a main body of a camera and a view finder, the invention may possibly be extended to providing a radio link between other parts of a video camera - e.g. a lens and signal processing unit in one part, and a recording and/or playback unit in another part.



CLAIMS

1. A radio transmitting circuit which is installed in a main body of a video camera having a detached view finder, the circuit comprising:

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a CCD portion for converting an image signal of an object input through a lens of said video camera into an electrical signal;

10 a preprocessor for receiving the electrical signal to perform an automatic white balance control, an automatic black balance control, a flare compensation, and a gamma compensation;

15 a video signal processor for receiving the preprocessed signal, performing a luminance/colour difference signal process, and outputting a composite video signal;

20 a synchronous signal separator for separating the composite video signal output from said video signal processor into vertical and horizontal synchronizing signals;

code means for encoding a code set through a keypad by a user to provide a code signal;

25 a timing controller for receiving the code signal output from said code means and overlapping the code signal on a predetermined horizontal synchronizing signal interval within the horizontal synchronizing signal separated in said synchronous signal separator;



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a mixer for mixing the overlapped signal of said timing controller and the video signal of said video signal processor;

5 a modulating portion for receiving the mixed signal from said mixer and modulating the received mixed signal by a carrier of a specific frequency; and

10 a transmitting portion for amplifying the modulated video signal of said modulator in an amplifier and then transmitting the amplified signal to said view finder through a transmitting antenna by radio.

2. A radio transmitting circuit as claimed in claim 1, wherein said timing controller comprises:

15 a counter for receiving and counting a horizontal synchronizing signal separated in said synchronous signal separator and outputting the result;

20 an A/D converter for receiving a clock signal from said counter to convert the analog vertical synchronizing signal detached in said synchronizing signal separator into a digital signal;

a memory for storing the converted digital signal in an assigned address in response to an address signal from the counter;

25 a read/write control logic portion for supplying a read/write logic signal to the memory in response to the output from said counter to read/write the vertical synchronizing signal stored in the memory;



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a D/A converter for converting the digital vertical synchronizing signal read and written in said memory according to the control signal of said read/write control logic portion, into an analog signal in response to a clock signal from said counter;

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a monostable multivibrator for delaying by a predetermined width the analog-converted vertical synchronizing signal from said D/A converter;

a gate circuit for gating an output from said counter and the output from said multivibrator and passing only a predetermined horizontal synchronizing signal;

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an AND gate for receiving and AND-gating the inverted signal of the output of said gate circuit and said video signal and outputting the logic result; and

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an adder for adding a horizontal synchronizing signal output from said AND gate to the output signals of said encoder.

3. A radio transmitting circuit as claimed in claim 1 or 2, wherein said code means comprises;

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a code generator for generating a code using the digits 0 through 9 input through said keypad by a user; and

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an encoder for encoding said code from said code generator to provide said code signals to be supplied to said timing controller.



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4. A radio receiving circuit of a video camera having a detached view finder in which said circuit is installed, said circuit comprising:

5 a receiving portion for receiving through a receiving antenna a signal transmitted by radio from a main body of said video camera, from which the view finder is detached;

a demodulator for amplifying and detecting the received signal supplied from said receiving portion;

10 a video signal processor for processing the detected video signal supplied from said demodulator;

a synchronous signal separator for separating said video signal into vertical and horizontal synchronizing signals;

15 a timing controller for extracting a code signal overlapped on a predetermined horizontal synchronizing signal interval separated in said synchronizing signal separator;

20 decoding means for comparing and discriminating the decoded signal of the code signal supplied from said timing controller and a predetermined code set through a keypad by a user;

25 a gating portion for passing or stopping the video signal supplied from said video signal processor in response to the signal supplied from said decoding means; and



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a display portion for receiving the video signal from said gating portion if passed thereby, amplifying the received video signal, separating a synchronizing signal, and then displaying a video signal on the screen of the view finder.

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5. A radio receiving circuit as claimed in claim 4, wherein said timing controller comprises:

10 a counter for receiving and counting the horizontal synchronizing signal separated in said synchronous signal separator and producing outputs;

an A/D converter for receiving a clock signal from said counter and converting an analog vertical synchronizing signal separated in said synchronous signal separator into a digital signal;

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a memory for storing the digital-converted signal into an assigned address in response to an address signal from said counter;

20 a read/write control logic portion for supplying a read/write logic signal to said memory in response to the output from said counter to read/write the vertical synchronizing signal stored in said memory;

25 a D/A converter for converting the digital vertical synchronizing signal read and written from said memory according to the control signal of said read/write control logic portion into an analog signal in response to a clock signal from said counter;



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a monostable multivibrator for delaying by a predetermined width the analog-converted vertical synchronizing signal from said D/A converter;

5 a gate circuit for gating an output from said counter and the output from said multivibrator and passing only a predetermined horizontal synchronizing signal; and

10 an AND gate for receiving and AND-gating the inverted signal of the output of said gate circuit and said video signal and outputting the logic result.

6. A radio receiving circuit as claimed in claim 4 or 5, wherein said decoding means comprises:

15 a code generator for generating a code using the digits 0 through 9 input through said keypad by a user;

20 a decoder for decoding a cryptic code loaded on the horizontal synchronizing signal of the video signal output from said timing controller; and

a code discriminator for receiving the output from said code generator and the output from said decoder and comparing and discriminating whether the two output signals match or not, and transmitting a corresponding signal to said gating portion.

25 7. A radio transmitting and/or receiving circuit of a video camera having a detached view finder, substantially as hereinbefore described with reference to Figures 1 and 2 of the accompanying drawings.



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8. A radio transmitting and/or receiving circuit of a video camera having a detached view finder, substantially as hereinbefore described with reference to Figures 1 and 6 of the accompanying drawings.
- 5 9. A video camera provided with a transmitting and/or receiving circuit according to any of the preceding claims.
- 10 10. A video camera comprising a plurality of parts contained in separate housings; a radio transmitter associated with one of said parts for transmitting video information from said one part; a radio receiver associated with another of said parts for receiving video information transmitted from said transmitter; and encoding means for setting first and second identifying codes for said transmitter and receiver respectively such that video information received by said receiver is fully processed only when said first code in a received signal
- 15 has a predetermined relationship with said second code.