Description

The present invention relates to a semiconductor integrated circuit device and a method of producing such a device.

Read Only Memories (ROMs) include a lateral mask ROM that is advantageous for high-speed operation and a vertical mask ROM that is advantageous for being highly densely integrated.

In a vertical mask ROM, a double-layer gate structure (multi-gate structure) has been employed for the purpose of accomplishing a highly dense integration. A vertical mask ROM of the double-layer gate structure has been disclosed in Japanese Patent Laid-Open No. 41188/1978.

The double-layer gate structure consists of second gate electrodes arranged among the first gate electrodes arranged in the direction of the gate length, maintaining a predetermined distance. The first gate electrodes are composed of a gate electrode material (e.g. polycrystalline silicon film) of a first layer, and the second gate electrodes are composed of a gate electrode material (polycrystalline silicon film) of a second layer. Ends of the first gate electrodes and ends of the second gate electrodes have been overlapped by amounts that correspond to margin for aligning the mask in the step of manufacturing.

Such a vertical mask ROM makes it possible to eliminate a portion that corresponds to the source region or the drain region between the first gate electrodes and the second gate electrodes. Thus, the vertical mask ROM of this type enables the areas of the memory cell array to be reduced in the direction of gate length and, hence, enables the degree of integration to be increased.

The data are written onto the vertical mask ROM prior to forming the first gate electrodes and the second gate electrodes. That is, the data are written onto the vertical mask ROM in a way as described below.

First, impurities for writing data are selectively introduced into the channel-forming regions in the main surface of a semiconductor substrate. The impurities for writing data form a depletion-type MISFET of a conductivity type opposite to that of the semiconductor substrate.

Then, first gate electrodes and second gate electrodes are formed in positions in a region where the impurites for writing data are introduced.

The inventor of the present invention has studied the devices discussed above and has found that they exhibit a number of problems.

In a vertical mask ROM in which the data have been written prior to forming the gate electrodes, extended periods of time are required for completing the product after the data have been written into the ROM.

An example of a vertical mask ROM is disclosed in JP-A-56-150858. In JP-A- 56-150858, the impurities are introduced before the electrodes are formed.

In such a vertical mask ROM, the first gate electrodes and the second gate electrodes must be formed in positions in the regions in which the impurities for writing data have been introduced. Therefore the gates in the direction of gate length, and/or the size of the region in which the impurities for writing data are introduced must have a margin to take into consideration the masking deviation between the region in which impurities for writing data are introduced and the first and second gate electrodes. Because of the above reasons, the degree of integration of the vertical mask ROM cannot be increased.

Furthermore, the masking deviation results in a deviation between the gates and the channel regions causing the gate length to be changed substantially. Therefore, the mutual conductance (gm) of a MISFET constituting a memory cell undergoes a change. Then, erroneous operation can take place in reading out the data. Variance in the mutual conductance (gm) that depends upon the manufacturing process causes the vertical mask ROM in which the memory cells are connected in series to operate erroneously.

Therefore, the present invention provides a method of producing a semiconductor integrated circuit read only memory device, comprising:

(a) a step of introducing first impurities into a surface of a semiconductor material having a first conductivity type, said impurities having a second conductivity type that is opposite to the first conductivity type;

(b) a step of forming gate insulating film on the surface of the semiconductor material;

(c) a step of forming on the gate insulating film a plurality of first conductive layers spaced apart by substantially equal lateral distances;

(d) after the steps (a), (b) and (c), a step of forming a plurality of second conductive layers among the plurality of first conductive layers on the gate insulating film in such a manner that the second conductive layers partly overlap the first conductive layers;

wherein the first and second conductive layers constitute gate electrodes of a plurality of MISFETs, said plurality of MISFETs being connected in series, wherein the threshold voltage of each of said plurality of MISFETs is adjusted to that of depletion type by the step (a);

(e) a step of selectively forming a masking layer above the first and second conductive layers; and

(f) a step of selectively introducing second impurities of the first conductivity type by using the masking layer as a mask for changing the threshold voltage of selected ones of said plurality of MISFETs from that of depletion type to that of enhancement type, wherein said second impurities are introduced through the first or second con-

ductive layers into the surface of the semiconductor material in such a manner that said second impurities are not introduced into the surface of the semiconductor material under portions where the first conductive layers and the second conductive layers overlap.

It can be noted that in JP-A-56-150860 there was a proposal to form all MISFETs, of depletion type prior to the formation of the electrodes, and subsequently introduce impurities to change some of those MISFETs to enhancement type in order to write data. However, JP-A-56-150860 was concerned with a lateral mask ROM and therefore there was no overlap of the electrodes and the MISFETs were laterally separated.

The present invention thus permits a device to be produced in a manner which is capable of reducing the time required from the writing of data to the completion of the product in a semiconductor integrated circuit device having vertical mask ROM.

The present invention also permits a device to be produced in a manner which is capable of reducing the areas occupied by the memory cells to increase the degree of integration in a semiconductor integrated circuit device having vertical mask ROM.

Furthermore, the present invention provides a technology by which it is possible to prevent the mutual conductance (gm) of MISFET that constitutes a memory cell from changing irrespective of the manufacturing processes for producing semiconductor integrated circuit devices having vertical mask ROM.

Thus, in a semiconductor integrated circuit device of the double-layer gate structure having vertical mask ROM, first gate electrodes and second gate electrodes are formed successively, and then impurities for writing data are introduced into a channel-forming region through a predetermined first gate and/or a second gate electrode thereby to write data.

Further, the impurities for writing data maybe introduced without passing through a portion where the end of the first gate electrode and the end of the second gate electrode overlap.

Embodiments of the invention will now be described in detail, by way of example, with reference to the accompanying drawings, in which:

Fig. 1 is a diagram of an equivalent circuit of a memory cell portion and a peripheral portion thereof in a vertical mask ROM produced by a process according to the present invention;

Fig. 2 is a plan view illustrating a major portion of the memory cell array in the vertical mask ROM;

Fig. 3 is a section view illustrating a major portion of the structure of a memory cell in the vertical mask ROM;

Figs. 4 to 8 are section views illustrating manufacturing steps in the method of producing the vertical mask ROM;

Figs. 9 and 10 illustrate another embodiment of a method of producing a vertical mask ROM;

Fig. 11 is a block diagram of a microcomputer on which is mounted the vertical mask ROM; and

Fig. 12 is a diagram showing on an enlarged scale the channels of MISFET's M_1 to M_4 of the memory cells.

Fig. 1 is a diagram of an equivalent circuit of a vertical mask ROM produced according to one embodiment of the present invention.

Referring to Fig. 1, a memory cell array in a vertical mask ROM has arranged therein memory cells M1 to M8 that are composed of MIS transistors or MISFET's (hereinafter simply referred to as MISFET's). The memory cells M1 to M8 are connected in series. Memory cells M1 to M8 of a number of eight (or 16,32 .....) form a unit memory cell row consisting of eight bits (or 16 bits, 32 bits, ... as appropriate).

The memory cell M consists of a MISFET of the depletion type (first threshold voltage) that forms data "0" or of the enhancement type (second threshold voltage) that forms data "1". Word lines WL that extend in a "column" direction are connected to the gate electrodes of the memory cells M1 to M8, such that the memory cells M may be rendered conductive or non-conductive by signals on the word lines WL. One end of each word line WL is connected to an X-decoder circuit Xdec.

The memory cell M1 in the unit memory cell row is connected to a data line DL that extends in a row direction. The drain of the MISFET of the memory cell M1 is connected to the data line DL that extends in the row direction, and the gate electrode thereof is connected to a power source voltage Vcc via a precharging MISFET Qpc that receives a precharge signal ϕpc. The power source voltage Vcc to operate the circuit may be, for example, 5 volts. The data lines DL are connected at the ends on one side to a common data line CD via MISFET's Qs that constitute column switches. The gate electrodes of MISFET's Qs are connected to a Y-decoder circuit Ydec. The source of the MISFET that forms memory cell M8 at the other end of the memory cell row is connected to a reference voltage Vss. The reference voltage Vss of the circuit is, for example, ground potential (0 volt). As will be described later, the power source voltage Vcc and the reference voltage Vss are provided in common for a plurality of unit memory cell rows that are arranged in the column direction, and forms wiring for power source voltage and wiring for reference voltage, respectively.

Each pair of unit memory cell rows forms a symmetrical shape in the row direction with the precharging MISFET Qpc as a centre. Each pair of unit memory cell rows are arranged in the column direction maintaining the same pattern to form the memory cell array.

Fig. 2 is a sectional view showing a major portion of the memory cell array in the vertical mask ROM,

and Fig. 3 is a sectional view along the line III-III in Fig. 2.

Referring to Figs. 2 and 3, the vertical mask ROM has a p^--type semiconductor substrate (or well region) 1 of single crystalline silicon. A field insulating film 2 and a p-type channel stopper region 3 are provided on the main surface between the semiconductor element-forming regions of the semiconductor substrate 1.

The vertical mask ROM include memory cells M_1, M_3, M_5, M_7 of odd-number columns constituted by the semiconductor substrate 1, a gate insulating film 4 and a gate electrode 5, and memory cells M_2, M_4, M_6, M_8 of even-number columns constituted by the semiconductor substrate 1, a gate insulating film 6 and a gate electrode 7. Thus, the memory cell has a MIS structure which contains neither a semiconductor region that corresponds to the source region nor a semiconductor region that corresponds to the drain region of MISFET.

The gate electrodes 5 of memory cells M of odd-numbered columns are arranged so that they maintain a predetermined distance (spacing) in the direction of gate length (direction of row in Fig. 2). The gate electrodes 5 are formed in a step of forming gate electrode of a first layer. The gate electrodes 5 are composed of, for example, a polycrystalline silicon film having a thickness of about 200 to 300 nm. Alternatively, the gate electrodes 5 may be composed of a single layer of a high-melting metal silicide ($MoSi_2$, WSi_2, $TaSi_2$, $TiSi_2$) film or of a high-melting metal (Mo, W, Ta, Ti) film, or may be composed of a composite film obtained by laminating a metal film on the polycrystalline silicon film. For example, when a polysilicide film is obtained by laminating a high-melting metal silicide film on a polycrystalline silicon film, the polycrystalline silicon film should have a thickness of from 150 to 200 nm and the high-melting metal silicide film should have a thicknesss of from 150 to 300 nm.

The gate electrodes 7 of memory cells M of even-number columns are arranged among the first gate electrodes 5. Ends of the gate electrodes 7 overlap the ends of the gate electrodes 5 by an amount that corresponds to a size of the masking margin (e.g. about 0.5 μm) in the step of forming the gate electrodes 5. The gate electrodes 7 are formed in a step of forming gate electrodes of a second layer. For instance, the gate electrodes 7 are composed of a material equivalent to that of the gate electrodes 5 and with a thickness substantially the same as that of the gate electrodes 5.

The gate electrodes 5 and the gate electrodes 7 are electrically isolated from each other by an interlayer insulating film (e.g. a silicon oxide film) that is not denoted by numeral but which is formed on the surface of the gate electrodes 5.

Data are written into memory cells M_3 and M_7 of the memory cells M of odd-numbered columns, and into memory cells M_2 and M_4 of the memory cells M of even-numbered columns. For the memory cells M into which data are written, impurities for writing data are introduced into the channel-forming region in the main surface of the semiconductor substrate 1 (in practice, this region is heat-treated to form a p-type semiconductor region). The memory cell M has been formed in advance (prior to writing data) by a threshold voltage of the depletion type; however, the threshold voltage is changed into the enhancement type by the introduction of impurities 9 for writing data.

The MISFET Qpc for selecting the above-mentioned eight stages of memory cells M is formed by the semiconductor substrate 1, gate insulating film 4, gate electrode 5 (or 7), and a pair of n^+-type semiconductor regions 8 used as a source region and a drain region. The memory cells M are formed by nearly the same step as the one for forming MISFET Qpc. The ground potential wiring Vss is formed by the semiconductor region 8.

A bit line 12 is connected to one semiconductor region 8 of the MISFET Qpc through a connection hole 11 formed in the interlayer insulating film 10. The interlayer insulating film 10 is formed, for example, by a composite film obtained by forming a BPSG film on a silicon oxide film formed by the CVD method. The bit line 12 is formed by an aluminium film, or a laminated film of an aluminium alloy to which Cu and/or Si are added and a high-melting metal silicide layer.

The method of producing such a vertical mask ROM, and the method of writing data, will now be described briefly in conjunction with Figs. 4 to 8 (sectional views showing each of the manufacturing steps).

First, a p^--type semiconductor substrate 1 composed of single crystalline silicon is prepared. The semiconductor substrate 1 has a surface concentration of about 1×10^{12} to 2×10^{12} atoms/cm^2.

Next, a field insulating film 2 and a p-type channel stopper region 3 are formed on the main surface between the semiconductor element-forming regions of the semiconductor substrate 1.

Then, impurities 13 for adjusting the threshold voltage are introduced into the main surface of the MISFET-forming region in the semiconductor substrate 1. The impurities 13 may be As^+ ions that are implanted in an amount of, for example, about 2×10^{12} to 3×10^{12} atoms/cm^2 at about 60 to 100 KeV. Owing to the introduction of impurities 13, the threshold voltage is adjusted to that of depletion type.

Referring to Fig. 4, a gate insulating film 4 is formed on the memory cell M-forming region and on the MISFET Qpc-forming region of the semiconductor substrate 1. The gate insulating film 4 is composed of a silicon oxide film formed by thermally oxidizing the main surface of the semiconductor substrate 1 at a temperature of 850° to 900°C, and has a thickness

of about 12.5 to 30 nm.

Referring to Fig. 5, gate electrodes (first gate electrodes) 5 are formed on predetermined portions on the gate insulating film 4 by the step of forming gate electrodes of the first layer. The gate electrodes 5, in this case, are composed of a single layer of polycrystalline silicon film. The polycrystalline silicon film is formed by a CVD method. Prior to subjecting the polycrystalline silicon film to the patterning to form gate electrodes, the phosphorus concentration therein is set to be about 1×10^{20} atoms/cm^{-3} by the treatment or implantation with phosphorus ions. Thereafter, the gate electrodes 5 are formed to form memory cells M of odd-number columns.

Next, the surface of the semiconductor substrate and the surface of the gate electrodes are thermally oxidized at 850° to 900°C to form a silicon oxide film on the surface of the semiconductor substrate maintaining a thickness of 12.5 to 30 nm and to form a silicon oxide film on the surface of gate electrodes maintaining a thickness of 100 to 200 nm. The oxidation is effected utilizing the fact that the rate of oxidation of the polycrystalline silicon film in which phosphorus ions are introduced is greater than that of the surface of the semiconductor substrate. A thick silicon oxide film is formed on the surfaces of gate electrodes because the silicon oxide film serves as a interlayer insulating film relative to the gate electrodes of the second layer to decrease the capacitance that is formed relative to the gate electrodes of the second layer.

Referring to Fig. 6, the gate electrodes (second gate electrodes) 7 are formed on the gate insulating film 6 by the step of forming gate electrodes of the second layer. The gate electrodes 7 are of polycrystalline silicon film in a manner as described above and have the same thickness as the gate electrodes of the first layer. Ends of the gate electrodes 7 overlap the ends of the gate electrodes 5 by an amount that corresponds to the size of masking margin in the manufacturing step. By forming the gate electrodes 7, memory cells M of even-number columns are formed.

After the gate electrodes are formed, the surfaces of gate electrodes and the surface of the semiconductor substrate are thermally oxidized to form silicon oxide films with thicknesses of about 50 nm and 10 to 20 nm, respectively.

Next, using the gate electrodes 5 and 7 as masks for introducing impurities, n^+-type semiconductor regions 8 are formed on the main surface of the semiconductor substrate 1 as shown in Fig. 7. The semiconductor regions 8 are formed by implanting As^+ ions or P^+ ions in amounts of 5×10^{15} to 1×10^{6} atoms/cm^2 at 80 KeV or 60 KeV. Owing to the formation of semiconductor regions 8, the MISFET Qpc for selecting memory cells is formed (similarly, a MISFET is also formed for constituting the peripheral circuit).

Next, the step of writing data is effected. First, a mask 14 is formed on the whole surfaces of the gate electrodes 5 and 7 to introduce impurities for writing data. The mask 14 for introducing data-writing impurities has openings 14A for exposing the surfaces of the gate electrodes 5 or the gate electrodes 7. As shown in Fig. 8, the inner walls of the opening 14A in the direction of gate length are so formed as will be positioned in a region (within the size of masking margin in a manufacturing step) in which an end of the gate electrode 5 and an end of the gate electrode 7 overlap each other. Further, the inner walls of the opening 14A in the direction of gate width are formed so that they are positioned on the outside of the gate width of the memory cell M by an amount at least corresponding to the size of masking margin in the manufacturing steps. The mask 14 for introducing the data-writing impurities is composed of, for example, a photoresist film.

Using the mask 14 for introducing data-wiring impurities as shown in Fig. 8, impurities 9 for writing data are selectively introduced into the channel-forming regions under the gate electrodes 5 or the gate electrodes 7 through gate electrodes 5 of memory cells M of odd-number columns or through gate electrodes 7 of memory cells M of even-number columns that are exposed through the openings 14A. The impurities 9 for writing data are composed of B^+ ions that are implanted at a concentration of about 7×10^{12} to 9×10^{12} atoms/cm^2 with the energy of about 140 to 160 KeV. When the gate electrodes are composed of a polysilicide, the energy for ion implantation is from 140 to 300 KeV. Under such conditions, a maximum concentration of impurities 9 for writing data can be set in the channel-forming regions under the gate electrodes 5 and/or the gate electrodes 7. The impurities 9 for writing data are not introduced into the main surface of the semiconductor substrate 1 under the portions where the ends of the gate electrodes 5 and the ends of the gate electrodes 7 overlap since the film at such portions has a large thickness. That is, the impurities 9 for writing data are defined by the mask 14 for introducing data-writing impurities and by the overlapped portions, and are introduced into the channel-forming regions in a self-aligned manner under the gate electrodes 5 and/or the gate electrodes 7. The impurities for writing data are activated by heat-treatment after they have been introduced. Introduction of impurities 9 for writing data changes the threshold voltage of the memory cell M from that of the depletion type to that of the enhancement type. The relationship between the impurity region 19 constituted by impurities for writing data activated by the heat-treatment after they have been introduced and the gate electrodes of the first and second layers will now be described with reference to Fig. 12. Fig. 12 illustrates MISFET's M_1 to M_4 which forms part of the memory cells. Here, the impurity region that is constituted by impurities that are introduced for forming

depletion-type MISFET's is not shown. To form MISFET's of the enhancement-type, ions are implanted from regions denoted by "L" in Fig. 12. Impurities implanted in the surface of the semiconductor substrate are diffused by heat-treatment for activation, i.e. diffused by an equal distance "w" in the direction of gate length. Referring, for example to MISFET M_3, both ends of the impurity region 19 are located at an equal distance in the direction of gate length from the ends of the gate electrode of the second layer. If an imaginary line c is presumed to exist midway between the ends of the neighbouring gate electrodes of the second layer, ends of the impurity layer 19 exist at positions on both sides of the imaginary line c being separated away therefrom by an equal distance B.

Thus, in a semiconductor integrated circuit device having a vertical mask ROM of the double-layer gate structure, the gate electrodes 5 and gate electrodes 7 are successively formed, impurities 9 are introduced into channel-forming regions through predetermined gate electrodes 5 and/or gate electrodes 7 to write data after the gate electrodes 5 and gate electrodes 7 have been formed. Therefore, the vertical mask ROM can be produced within reduced periods of time, as compared to known devices.

Further, impurities 9 for writing data are introduced without passing through portions where the ends of the gate electrodes 5 and the ends of the gate electrodes 7 are overlapped. Thus, since they are defined by the overlapped regions, the impurities 9 for writing data are introduced into the channel-forming regions under predetermined gate electrodes 5 and/or gate electrodes 7 only. Thus, the impurities 9 for writing data are introduced in a way that ensures they are self-aligned to the gate electrodes 5 and/or the gate electrodes 7. Hence, the area of the memory cell M can be reduced in the direction of gate length, enabling the integration degree of the vertical mask ROM to be increased.

The channel length of a MISFET, e.g. M_3 constituted by the gate electrodes of the first layer is determined by a distance between the gate electrodes of MISFET's M_2 and M_4. Therefore, the channel length does not change irrespective of the masking deviation; i.e., a constant channel length is obtained. In other words, a constant mutual conductance (gm) is obtained at all times.

The channel length of a MISFET, e.g. M_2 formed by the gate electrodes of the second layer is determined by a distance between the gate electrodes of the MISFET's M_1 and M_3. Therefore, a MISFET having a constant mutual conductance (gm) is obtained as described above.

After the step of writing data, the mask 14 for introducing the data-writing impurities is removed.

Then, an SiO_2 film is formed maintaining a thickness of 150 nm and a BPSG (boron phosphosilicate glass) film is formed, maintaining a thickness of 40 nm by a CVD method in order to form successively an interlayer insulating film 10 and connection holes 11. Thereafter, bit lines 12 are formed as shown in Figs. 2 and 3, and a plasma nitride film is formed thereon maintaining a thickness of 1.2 μm to complete the vertical mask ROM of the double-layer gate structure in accordance with the embodiment. The bit lines are comprised of a molybdenum silicide film having a thickness of 15 to 30 nm and an aluminium film having a thickness of 800 nm formed thereon.

In the vertical mask ROM produced by the method of the present invention, the step of writing data may be carried out after the interlayer insulating film 10 or the bit line 12 has been formed. Described below is an embodiment in which the step of writing data is executed after the bit lines 12 have been formed.

After the steps have been finished the stage shown in Fig. 7 in the embodiment discussed above, an interlayer insulating film composed of CVD-SiO_2 of a thickness of about 150 nm and BPSG of a thickness of about 400 nm is formed as shown in Fig. 9 without effecting the step of writing data. Then, a connection hole 11 is formed in the drain region of MISFET Qpc. Thereafter, there are formed bit lines of a molybdenum silicide film having a thickness of 15 to 30 nm and an aluminium film that contains Cu and Si having a thickness of 800 nm is formed thereon. Further, a protection film composed of silane is formed by the CVD method maintaining a thickness of 100 to 200 nm. Like Fig. 3, Fig. 9 is a section view along the line III-III of Fig. 2.

Next, the mask 14 for introducing data-writing impurities is formed on the protection film 15. Referring to Fig. 10, the impurities 9 for writing data are introduced into the channel-forming regions of predetermined memory cells M through openings 14A in the mask 14 thereby to write data. The data are written by implanting, for example, B^+ ions at a concentration of about 7×10^{12} to 9×10^{12} atoms/cm^2 with the energy of about 300 KeV. The mask 14 for introducing impurities for writing data is composed of a photoresist film.

The protection film 15 is formed so as to withstand washing in the steps of applying a photoresist film, developing and peeling, as well as to withstand wet processing such as treatment with a developing solution and treatment with a peeling solution. That is, the protection film 15 is formed such that the bit lines 13 (of aluminium or an alloy thereof) will not be corroded.

In particular, when copper is added to the bit lines 13 to decrease migration thereof, corrosion easily takes place in the aluminium alloy. The protection film of the present invention is particularly effective for the vertical mask ROM that uses aluminium alloy containing copper.

The protection film is not limited to a silane film only, bit may be, for example, a nitride film or a polycrystalline silicon film.

After the data are written, the mask 14 for introducing the data-writing impurities is removed. Next, a passivation film composed, for example, of a plasma nitride film is formed maintaining a thickness of about 1.2 μm on the protection film 15. Thereafter, the data-writing impurities 9, introduced in the step of writing the data, are activated.

According to this embodiment, the time for completing the product mentioned in the foregoing embodiment can be further shortened.

Fig. 11 is a block diagram of a microcomputer to which the vertical mask ROM produced by the method of the present invention is adapted.

In Fig. 11 there is shown a semiconductor substrate (chip) 17 composed of p^--type single crystalline silicon having a plurality of bonding pads 18 arranged around the periphery thereof. An input/output circuit region I/O is provided on the inside of the bonding pads 18. The chip 17 shown in Fig. 11 contains a micro ROM, a CPU (central processing unit), an SCI (serial communication interface), an A/D (analog-digital converter) circuit, a dual-RAM (dual port random access memory), a RAM, a ROM, a timer 1, a timer 2 and a timer 3.

With the vertical ROM produced by the method of the present invention being adapted to the micro ROM and or ROM, the time can be reduced from the step of writing data to the completion of the product.

Claims

1. A method of producing a semiconductor integrated circuit read only memory device, comprising:
   (a) a step of introducing first impurities (13) into a surface of a semiconductor material (1) having a first conductivity type, said impurities (13) having a second conductivity type that is opposite to the first conductivity type;
   (b) a step of forming gate insulating film (4,6) on the surface of the semiconductor material (1);
   (c) a step of forming on the gate insulating film (4) a plurality of first conductive layers (5) spaced apart by substantially equal lateral distances;
   (d) after the steps (a), (b) and (c), a step of forming a plurality of second conductive layers (7) among the plurality of first conductive layers (5) on the gate insulating film (6) in such a manner that the second conductive layers (7) partly overlap the first conductive layers (5);
   wherein the first and second conductive layers (5,7) constitute gate electrodes of a plurality of MISFETs, said plurality of MISFETs being connected in series, wherein the threshold voltage of each of said plurality of MISFETs is adjusted to that of depletion type by the step (a);
   (e) a step of selectively forming a masking layer (14) above the first and second conductive layers (5,7); and
   (f) a step of selectively introducing second impurities (9) of the first conductivity type by using the masking layer (14) as a mask for changing the threshold voltage of selected ones of said plurality of MISFETs from that of depletion type to that of enhancement type, wherein said second impurities (9) are introduced through the first or second conductive layers (5,7) into the surface of the semiconductor material (1) in such a manner that said second impurities (9) are not introduced into the surface of the semiconductor material (1) under portions where the first conductive layers (5) and the second conductive layers (7) overlap.

2. A method according to claim 1, additionally comprising:
   (g) a step of forming a first insulating film (10) on the semiconductor material (1) and on the first and second conductive layers (5,7);
   (h) a step of selectively forming a third conductive layer (12) on the first insulating film (10);
   (i) a step of forming a second insulating film (15) on the third conductive layer (12) and on the first insulating film (10),
   wherein steps (g), (h) and (i) are carried out before steps (e) and (f), and
   wherein the masking layer (14) is formed on the second insulating film (15); and
   (j) a step of selectively removing the masking layer (14) using the second insulating film (15) as an etching-preventing film.

3. A method according to claim 2, wherein the step of forming the first insulating film (10) consists of a step of forming a silicon oxide film and a step of forming a BPSG.

4. A method according to claim 2 or claim 3, wherein the step of forming the third conductive layer (12) consists of a step of forming a high-melting metal silicide layer and a step of forming an aluminium alloy layer.

5. A method according to any one of the preceding claims, wherein the masking layer (14) has openings (14A) at positions corresponding to selected ones of the plurality of first conductive layers (5) and/or the plurality of second conductive layers (7), and said second impurities (9) of the first conductivity type are introduced into the openings.

After the data are written, the mask 14 for introducing the data-writing impurities is removed. Next, a passivation film composed, for example, of a plasma nitride film is formed maintaining a thickness of about 1.2 μm on the protection film 15. Thereafter, the data-writing impurities 9, introduced in the step of writing the data, are activated.

According to this embodiment, the time for completing the product mentioned in the foregoing embodiment can be further shortened.

Fig. 11 is a block diagram of a microcomputer to which the vertical mask ROM produced by the method of the present invention is adapted.

In Fig. 11 there is shown a semiconductor substrate (chip) 17 composed of p^--type single crystalline silicon having a plurality of bonding pads 18 arranged around the periphery thereof. An input/output circuit region I/O is provided on the inside of the bonding pads 18. The chip 17 shown in Fig. 11 contains a micro ROM, a CPU (central processing unit), an SCI (serial communication interface), an A/D (analog-digital converter) circuit, a dual-RAM (dual port random access memory), a RAM, a ROM, a timer 1, a timer 2 and a timer 3.

With the vertical ROM produced by the method of the present invention being adapted to the micro ROM and or ROM, the time can be reduced from the step of writing data to the completion of the product.

Claims

1. A method of producing a semiconductor integrated circuit read only memory device, comprising:
   (a) a step of introducing first impurities (13) into a surface of a semiconductor material (1) having a first conductivity type, said impurities (13) having a second conductivity type that is opposite to the first conductivity type;
   (b) a step of forming gate insulating film (4,6) on the surface of the semiconductor material (1);
   (c) a step of forming on the gate insulating film (4) a plurality of first conductive layers (5) spaced apart by substantially equal lateral distances;
   (d) after the steps (a), (b) and (c), a step of forming a plurality of second conductive layers (7) among the plurality of first conductive layers (5) on the gate insulating film (6) in such a manner that the second conductive layers (7) partly overlap the first conductive layers (5);
   wherein the first and second conductive layers (5,7) constitute gate electrodes of a plurality of MISFETs, said plurality of MISFETs being connected in series, wherein the threshold voltage of each of said plurality of MISFETs is adjusted to that of depletion type by the step (a);
   (e) a step of selectively forming a masking layer (14) above the first and second conductive layers (5,7); and
   (f) a step of selectively introducing second impurities (9) of the first conductivity type by using the masking layer (14) as a mask for changing the threshold voltage of selected ones of said plurality of MISFETs from that of depletion type to that of enhancement type, wherein said second impurities (9) are introduced through the first or second conductive layers (5,7) into the surface of the semiconductor material (1) in such a manner that said second impurities (9) are not introduced into the surface of the semiconductor material (1) under portions where the first conductive layers (5) and the second conductive layers (7) overlap.

2. A method according to claim 1, additionally comprising:
   (g) a step of forming a first insulating film (10) on the semiconductor material (1) and on the first and second conductive layers (5,7);
   (h) a step of selectively forming a third conductive layer (12) on the first insulating film (10);
   (i) a step of forming a second insulating film (15) on the third conductive layer (12) and on the first insulating film (10),
   wherein steps (g), (h) and (i) are carried out before steps (e) and (f), and
   wherein the masking layer (14) is formed on the second insulating film (15); and
   (j) a step of selectively removing the masking layer (14) using the second insulating film (15) as an etching-preventing film.

3. A method according to claim 2, wherein the step of forming the first insulating film (10) consists of a step of forming a silicon oxide film and a step of forming a BPSG.

4. A method according to claim 2 or claim 3, wherein the step of forming the third conductive layer (12) consists of a step of forming a high-melting metal silicide layer and a step of forming an aluminium alloy layer.

5. A method according to any one of the preceding claims, wherein the masking layer (14) has openings (14A) at positions corresponding to selected ones of the plurality of first conductive layers (5) and/or the plurality of second conductive layers (7), and said second impurities (9) of the first conductivity type are introduced into the openings.

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6. A method according to any one of the preceding claims, further comprising:

a step of introducing further impurities (8) having the second conductivity type into ends of both sides of the first and second conductive layers that are continuously formed using said first or second conductive layers as masks, after step (d) has been completed.

7. A method according to any one of the preceding claims, wherein the second conductive layers (7) are formed in such a manner that the second conductive layers (7) have substantially the same film thickness as that of the first conductive layers (5).

8. A method according to any one of the preceding claims, wherein the first conductivity type is p-type, and the second conductivity type is n-type.

Patentansprüche

1. Verfahren zur Herstellung eines Halbleiter-Festspeichers in integrierter Schaltungstechnik, umfassend

(a) einen Schritt, in dem in eine Oberfläche eines Halbleitermaterials (1) eines ersten Leitfähigkeitstyps erste Störstoffe (13) eines zu dem ersten Leitfähigkeitstyp entgegengesetzten zweiten Leitfähigkeitstyps eingebracht werden,

(b) einen Schritt, in dem auf der Oberfläche des Halbleitermaterials (1) ein Gate-Isolierfilm (4, 6) ausgebildet wird,

(c) einen Schritt, in dem auf dem Gate-Isolierfilm (4) mehrere erste Leiterschichten (5) in im wesentlichen gleichen seitlichen Abständen voneinander aufgebracht werden,

(d) einen nach den Schritten (a), (b) und (c) ausgeführten Schritt, in dem bei den mehreren ersten Leiterschichten (5) auf dem Gate-Isolierfilm (6) mehrere zweite Leiterschichten (7) derart erzeugt werden, daß sie die ersten Leiterschichten (5) teilweise überlappen,

wobei die ersten und die zweiten Leiterschichten (5, 7) Gate-Elektroden mehrerer in Reihe geschalteter MISFETs bilden und die Schwellenspannung jedes dieser MISFETs durch den Schritt (a) auf diejenige des Verarmungstyps eingestellt wird,

(e) einen Schritt, in dem über den ersten und den zweiten Leiterschichten (5, 7) eine Maskierschicht (14) selektiv ausgebildet wird, und

(f) einen Schritt, in dem unter Verwendung der Maskierschicht (14) als Maske zweite Störstoffe (9) des ersten Leitfähigkeitstyps selektiv eingebracht werden, um die Schwellenspannung ausgewählter der mehreren MISFETs von der des Verarmungstyps in die des Anreicherungstyps zu ändern, wobei die zweiten Störstoffe (9) durch die ersten und die zweiten Leiterschichten (5, 7) derart in die Oberfläche des Halbleitermaterials (1) eingebracht werden, daß die zweiten Störstoffe (9) in die Oberfläche des Halbleitermaterials (1) unter solchen Teilen nicht eingebracht werden, wo die ersten und die zweiten Leiterschichten (5, 7) einander überlappen.

2. Verfahren nach Anspruch 1, ferner umfassend

(g) einen Schritt, in dem auf dem Halbleitermaterial (1) sowie auf den ersten und den zweiten Leiterschichten (5, 7) ein erster Isolierfilm (10) ausgebildet wird,

(h) einen Schritt, in dem auf dem ersten Isolierfilm (10) eine dritte Leiterschicht (12) selektiv ausgebildet wird,

(i) einen Schritt, in dem auf der dritten Leiterschicht (12) und dem ersten Isolierfilm (10) ein zweiter Isolierfilm (15) ausgebildet wird,

wobei die Schritte (g), (h) und (i) vor den Schritten (e) und (f) ausgeführt werden, und

wobei die Maskierschicht (14) auf dem zweiten Isolierfilm (15) ausgebildet wird, und

(j) einen Schritt, in dem die Maskierschicht (14) unter Verwendung des zweiten Isolierfilms (15) als Ätzverhinderungsfilm selektiv entfernt wird.

3. Verfahren nach Anspruch 2, wobei der Schritt, in dem der erste Isolierfilm (10) ausgebildet wird, aus einem Schritt besteht, in dem ein Siliziumoxidfilm erzeugt wird, sowie aus einem Schritt, in dem ein BPSG-Film erzeugt wird.

4. Verfahren nach Anspruch 2 oder 3, wobei der Schritt, in dem die dritte Leiterschicht (12) ausgebildet wird, aus einem Schritt besteht, in dem eine hochschmelzende Metallsilicid-Schicht erzeugt wird, sowie aus einem Schritt, in dem eine Aluminiumlegierungs-Schicht erzeugt wird.

5. Verfahren nach einem der vorhergehenden Ansprüche, wobei die Maskierschicht (14) an Stellen, die ausgewählten der mehreren ersten Leiterschichten (5) und/oder der mehreren zweiten Leiterschichten (7) entsprechen, Öffnungen aufweist und die zweiten Störstoffe (9) des ersten Leitfähigkeitstyps in die Öffnungen eingebracht werden.

6. Verfahren nach einem der vorhergehenden Ansprüche, umfassend

einen Schritt, in dem nach Abschluß des

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Schrittes (d) in Enden an beiden Seiten der ersten und der zweiten Leiterschichten weitere Störstoffe (8) des zweiten Leitfähigkeitstyps eingebracht werden, die unter Verwendung der ersten und der zweiten Leiterschichten als Masken kontinuierlich ausgebildet werden.

7. Verfahren nach einem der vorhergehenden Ansprüche, wobei die zweiten Leiterschichten (7) derart erzeugt werden, daß sie im wesentlichen die gleiche Filmdicke wie die ersten Leiterschichten aufweisen.

8. Verfahren nach einem der vorhergehenden Ansprüche, wobei der erste Leitfähigkeitstyp der p-Typ und der zweite Leitfähigkeitstyp der n-Typ ist.

Revendications

1. Procédé pour produire un dispositif de mémoire morte à circuits intégrés à semiconducteurs, comprenant :
   (a) une étape d'introduction de premières impuretés (13) dans une surface d'un matériau semiconducteur (1) possédant un premier type de conductivité, lesdites impuretés (13) possédant un second type de conductivité qui est opposé au premier type de conductivité;
   (b) une étape de formation d'une pellicule isolante de grille (4,6) sur la surface du matériau semiconducteur (1);
   (c) une étape de formation, sur la pellicule isolante de grille (4), d'une pluralité de premières couches conductrices (5) séparées par des distances latérales sensiblement égales;
   d) après les étapes (a), (b) et (c), une étape de formation d'une pluralité de secondes couches conductrices (17) entre la pluralité de premières couches conductrices (5) sur la pellicule isolante de grille (6) de telle sorte que les secondes couches conductrices (7) chevauchent partiellement les premières couches conductrices (5);
   les première et seconde couches conductrices (5, 7) constituant des électrodes de grille d'une pluralité de transistors MISFET, ladite pluralité de transistors MISFET étant branchés en série, et la tension de seuil de chaque transistor de ladite pluralité de transistors MISFET étant réglée sur celle du type à appauvrissement au moyen de l'étape (a);
   (e) une étape de formation sélective d'une couche de masquage (14) au-dessus des première et seconde couches conductrices (5, 7); et
   (f) une étape d'introduction sélective de secondes impuretés (9) possédant le premier type de conductivité en utilisant la couche de masquage (14) en tant que masque pour commuter la tension de seuil de transistors sélectionnés faisant partie de ladite pluralité de transistors MISFET de celle du type à appauvrissement à celle du type à enrichissement, lesdites secondes impuretés (9) étant introduites à travers les premières ou secondes couches conductrices (5, 7) dans la surface du matériau semiconducteur (1) de telle sorte que lesdites secondes impuretés (9) ne sont pas introduites dans la surface du matériau semiconducteur (1), au-dessous de parties dans lesquelles les premières couches conductrices (5) et les secondes couches conductrices (7) se chevauchent.

2. Procédé selon la revendication 1, comprenant en outre :
   (g) une étape de formation d'une première pellicule isolante (10) sur le matériau semiconducteur (1) et sur les premières et secondes couches conductrices (5, 7);
   (h) une étape de formation sélective d'une troisième couche conductrice (12) sur la première pellicule isolante (10);
   (i) une étape de formation d'une seconde pellicule isolante (15) sur la troisième couche conductrice (12) et sur la première pellicule isolante (10),
   les étapes (g), (h) et (i) étant exécutées avant les étapes (e) et (f), et
   la couche de masquage (14) étant formée sur la seconde pellicule isolante (15); et
   (j) une étape d'élimination sélective de la couche de masquage (14) moyennant l'utilisation de la seconde pellicule isolante (15) en tant que pellicule empêchant la corrosion.

3. Procédé selon la revendication 2, dans lequel l'étape de formation de la première pellicule isolante (10) est constituée par une étape de formation d'une pellicule d'oxyde de silicium et une étape de formation de verre de borophosphosilicate.

4. Procédé selon la revendication 2 ou 3, dans lequel l'étape de formation de la troisième couche conductrice est constituée par une étape de formation d'une couche de siliciure métallique à point de fusion élevé et une étape de formation d'une couche d'alliage d'aluminium.

5. Procédé selon l'une quelconque des revendications précédentes, dans lequel la couche de masquage (14) possède des ouvertures (14A) en des positions qui correspondent à des couches sélec-

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tionnées faisant partie de la pluralité de premières couches conductrices (5) et/ou de la pluralité de secondes couches conductrices (7), et lesdites secondes impuretés (9) possédant le premier type de conductivité sont introduites dans les ouvertures.

6. Procédé selon l'une quelconque des revendications précédentes, comprenant en outre : une étape d'introduction d'autres impuretés (8) possédant le second type de conductivité dans des extrémités des deux faces des première et seconde couches conductrices, qui sont formées continûment en utilisant lesdites premières ou secondes couches conductrices en tant que masques, une fois exécutée l'étape (d).

7. Procédé selon l'une quelconque des revendications précédentes, dans lequel les secondes couches conductrices (7) sont réalisées de telle sorte que les secondes couches conductrice (7) possèdent sensiblement la même épaisseur que celle des premières couches conductrices (5).

8. Procédé selon l'une quelconque des revendications précédentes, dans lequel le premier type de conductivité est le type p et le second type de conductivité est le type n.

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