

Description

The invention generally relates to balanced filter circuits. Such circuits are known from US PS 4,509,019 and are composed of a number of balanced amplifiers having inverting and non-inverting inputs and outputs, which are coupled to each other via resistors and/or capacitors. The manner in which this coupling is effected and the values of the resistors and capacitors are determinative of the shape and the order of the transfer function from the inputs to the outputs of the filter circuit. In the known balanced filter circuits, the number of balanced amplifiers increases with the order of the transfer function of the filter circuit. For filter circuits of higher order the complexity of the circuit consequently rapidly increases.

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The invention has for its object to provide a balanced filter circuit having a composition which is simple even with a higher order of the transfer function.

According to the invention, this object is achieved by a balanced filter circuit having an Nth order transfer function H_N from a balanced input signal to a balanced output signal, N being an integer larger than or equal to two, comprising:

- a first and a second filter input for supplying the balanced input signal;
- a first and a second filter output for deriving the balanced output signal;
- only one balanced amplifier having an inverting and a non-inverting input and an inverting output coupled to the first filter output and a non-inverting output coupled to the second filter output;
- at least one of a first, a second, a third and a fourth pair of admittances of a first and a second admittance,

the first admittance of the first pair of admittances being connected between the first filter input and the inverting input and the second admittance being connected between the second filter input and the non-inverting input, the first admittance of the second pair of admittances being connected between the first filter input and the non-inverting input and the second admittance being connected between the second filter input and the inverting input, the first admittance of the third pair of admittances being connected between the inverting output and the non-inverting input and the second admittance being connected between the non-inverting output and the inverting input and the first admittance of the fourth pair of admittances being connected between the inverting output and the inverting input and the second admittance being connected between the non-inverting output and the non-inverting input.

According to the invention, each balanced filter circuit of the second order or of a higher order can be realized with only one amplifier. As a result, from the order two a very simple filter configuration is obtained. Due to the fact that this configuration comprises only one amplifier, the filter circuits according to the invention require only a limited number of electronic components, which permits an integration on a comparatively small surface.

The invention is based on the recognition of the fact that the transfer from the input signal U_{in} to the output signal U_{out} of each linear filter circuit can be written as:

$$\frac{U_{out}}{U_{in}} = \frac{Y1(P) - Y2(P)}{Y3(P) - Y4(P)}$$

P representing the complex frequency and $Y1(P)$, $Y2(P)$, $Y3(P)$ and $Y4(P)$ being the complex admittances of a first and a second positive admittance of four pairs of admittances. Further, each of the four admittances $Yi(P)$ can be described as a series of the type:

$$Yi(P) = a + b \cdot P + \sum_K (P \cdot A_K / (P + B_K))$$

in which a , b , A_K and B_K are real non-negative numbers. The term a represents the admittance of a resistor having a value $1/a$, while the term $b \cdot P$ represents the admittance of a capacitor having a value b and each of the terms of the sum $\sum$ represent the admittance of a series-combination of a resistor having a value $1/A_K$ and a capacitor having a value A_K/B_K . The admittances Yi can be realized with resistors and capacitors and when connected to the inputs and outputs of one balanced amplifier they yield a transfer function of the aforementioned type. Negative coefficients in the transfer function are discounted in the admittances $Y2$ and $Y4$, which are connected in cross-coupling with respect to the admittances $Y1$ and $Y3$ to the inputs of the amplifier.

A first embodiment of a balanced filter circuit according to the invention is characterized in that the filter circuit has a second order transfer function having the shape:

$$H2 = \frac{M \cdot P \cdot Wo / Qo}{P \cdot P + P \cdot Wo / Qo + Wo \cdot Wo}$$

in which

P = complex frequency,
Wo = resonance frequency,
Qo = Q factor and $Qo > 1/2$,

M = amplification factor,
and

- the first and the second admittance of the second pair of admittances each comprise a series-combination of a first resistor having a value substantially equal to $K \cdot Q_0 / W_0 / M$ and a first capacitor having a value substantially equal to $M \cdot W_0 / (Q_0 \cdot a \cdot K)$;
- the first and the second admittance of the third pair of admittances each comprise a parallel-combination of a second resistor having a value substantially equal to $K \cdot a / (W_0 \cdot W_0)$ and a capacitor having a value substantially equal to $1/K$;
- the first and the second admittance of the fourth pair of admittances each comprise a series-combination of a third resistor having a value substantially equal to $-K / (-a + W_0 / Q_0 - W_0 \cdot W_0)$ and a third capacitor having a value substantially equal to $-(-a + W_0 / Q_0 - W_0 \cdot W_0) / (a \cdot K)$,

a and K being positive real numbers. This filter circuit is a resonance circuit, which is particularly suitable for use in selective amplifiers.

With the choice of $a = W_0$, a second embodiment of a balanced filter circuit according to the invention is obtained, which is characterized in that

- the first and the second admittance of the second pair of admittances each comprise the series-combination of a first resistor having a value substantially equal to $Q_0 \cdot R / M$ and a first capacitor having a value substantially equal to $M \cdot C / Q_0$;
- the first and the second admittance of the third pair of admittances each comprise the parallel-combination of a second resistor having a value substantially equal to R, a second capacitor having a value substantially equal to C and a series-combination of a third resistor having a value substantially equal to $Q_0 \cdot R$ and a third capacitor having a value substantially equal to C / Q_0 ;
- the first and the second admittance of the fourth pair of admittances each comprise a series-combination of a fourth resistor having a value substantially equal to $R/2$ and a fourth capacitor having a value substantially equal to $2 \cdot C$,

R and C being constants to be chosen, for which it holds that: $R \cdot C = 1 / W_0$. In this second embodiment, the filter parameters resonance frequency W_0 and Q factor Q_0 are directly present in the element values, which is of importance if one of these parameters should be regulated. The embodiment is moreover particularly suitable for low values of Q_0 , at which the spread of the element values, i.e. the ratio between the largest and the smallest value, is not excessively large.

A third embodiment of a balanced filter circuit according to the invention is characterized in that the filter circuit has a second order transfer function having the shape:

$$H_2 = \frac{P \cdot P - P \cdot W_0 / Q_0 + W_0 \cdot W_0}{P \cdot P + P \cdot W_0 / Q_0 + W_0 \cdot W_0} \cdot M$$

in which

P = complex frequency,
W₀ = resonance frequency,
Q₀ = Q factor of $Q_0 \geq 1/2$,
M = amplification factor,

and

- the first and the second admittance of the first pair of admittances each comprise a parallel-combination of a first resistor having a value substantially equal to R/M and a first capacitor having a value substantially equal to $M \cdot C$;
- the first and the second admittance of the second pair of admittances each comprise a parallel-combination of a series-combination of a second resistor having a value substantially equal to $R/(2 \cdot M)$ and a second capacitor having a value substantially equal to $2 \cdot M \cdot C$ and a series-combination of a third resistor having a value substantially equal to $Q_0 \cdot R/M$ and a third capacitor having a value substantially equal to $M \cdot C / Q_0$;
- the first and the second admittance of the third pair of admittances each comprise a parallel-combination of a fourth resistor having a value substantially equal to R, a fourth capacitor having a value substantially equal to C and a series-combination of a fifth resistor having a value substantially equal to $R/2$ and a fifth capacitor having a value substantially equal to $2 \cdot C$;
- the first and the second admittance of the fourth pair of admittances each comprise a series-combination of a sixth resistor having a value substantially equal to $Q_0 \cdot R$ and a sixth capacitor having a value substantially equal to C / Q_0 ,

R and C being constants to be chosen, for which it holds that $R \cdot C = 1 / W_0$. This filter circuit is an all-pass network and due to its simplicity it is particularly suitable for group delay correction of filters which otherwise could be

corrected only by means of comparatively complicated circuits.

A fourth embodiment of a balanced filter circuit according to the invention is characterized in that the filter circuit has a third order transfer function having the shape:

$$H_3 = \frac{(P^2 P - a^* P + b)(P - c)}{(P^2 P + a^* P + b)(P + c)} \cdot M$$

in which

P = complex frequency,

a, b, c = a real positive number larger than zero and $a^* a < 4 \cdot b$

M = amplification factor

and

- the first and the second admittance of the first pair of admittances each comprise a parallel-combination of a first capacitor having a value substantially equal to M/K and the series-combination of a first resistor having a value substantially equal to $K/A/M$ and a second capacitor having a value substantially equal to $M \cdot A/(c \cdot K)$
- the first and the second admittance of the second pair of admittances each comprise a parallel-combination of a second resistor having a value substantially equal to $K/M \cdot b/d$ and a series-combination of a third resistor having a value substantially equal to $-K/B/M$ and a third capacitor having a value substantially equal to $-B \cdot M/(d \cdot K)$;
- the first and the second admittance of the third pair of admittances each comprise a parallel-combination of a fourth resistor having a value substantially equal to $K \cdot b/d$ and a capacitor having a value substantially equal to $1/K$;
- the first and the second admittance of the fourth pair of admittances each comprise a series-combination of a fifth resistor having a value substantially equal to $-K/C$ and a fifth capacitor having a value substantially equal to $-C/(d \cdot K)$,

in which d is a positive real number larger than c ,

$$A = 2 \cdot (c^2 + a^* c + b)/(d - c)$$

$$B = -(d + a + b/d)(d + c)/d - c)$$

$$C = -(d - a + b/d)$$

and K is a positive real number.

This filter circuit is an all-pass network which is particularly suitable for use as a section of a delay line having taps, the low Q factor of the complex pole pair being advantageous with the implementation with one amplifier.

The invention will be described more fully with reference to the accompanying drawing, in which:

Fig. 1 shows a known balanced band-pass filter circuit of the second order,

Fig. 2 shows circuit diagrams for the explanation of the operation of balanced filter circuits according to the invention,

Fig. 3 shows a first embodiment of a second order balanced band-pass filter circuit according to the invention,

Fig. 4 shows a second embodiment of a second order balanced band-pass filter circuit according to the invention,

Fig. 5 shows an embodiment of a second order all-pass balanced filter circuit according to the invention,

Fig. 6 shows a second embodiment of a second order all-pass balanced filter circuit according to the invention,

Fig. 7 shows an embodiment of a third order all-pass balanced filter circuit according to the invention,

Fig. 8 shows examples of equivalent admittances for use in a balanced filter circuit according to the invention, and

Fig. 9 shows an RC-ladder-type network for use in a balanced filter circuit according to the invention.

Fig. 1 shows a known balanced filter circuit. The circuit comprises two balanced amplifiers 10, 20 each having a non-inverting input 5, an inverting input 6, an inverting output 7 and a non-inverting output 8. The inputs 5, 6 are connected via resistors and/or capacitors to filter inputs 1, 2 of the filter circuit and/or to the outputs of the same amplifier and/or the outputs of one or more other amplifiers. The outputs 7, 8 of one of the amplifiers, in this case those of the amplifier 10, are connected to the filter outputs 3, 4. The signal U_{in} to be filtered is supplied in balanced form as $+U_{in}/-U_{in}$ at the filter inputs 1, 2. The filtered signal is available in balanced form as $-U_{out}/+U_{out}$ at the filter outputs 3, 4. The configuration of the circuit determines the transfer function U_{out}/U_{in} of the filter. This transfer function can be written as the ratio between a numerator polynomial $N(P)$ and a denominator polynomial $D(P)$ of the complex frequency P with real coefficients:

$$\frac{U_{out}}{U_{in}} = \frac{N(P)}{D(P)} \quad (1)$$

The highest of the degrees of numerator and denominator polynomials determines the order of the transfer function. The filter circuit of Fig. 1 has a transfer function of the order 2 and behaves like a second order band-pass filter. In the known filter circuit, the number of balanced amplifiers is equal to the order of the transfer function of the filter. This generally holds for balanced filter circuits known hitherto, so not only for the second order filter circuit of Fig. 1. From the order 2 the filter design can be simplified with a balanced filter circuit according to the invention because by means of this circuit any filter type of any order can be realized with only one balanced amplifier. The single amplifier on the one hand permits a small supply current consumption of the filter circuit. On the other hand, the supply current available, which in the known filter circuits must be distributed over several amplifiers, can now be fully utilized for the single amplifier. This single amplifier can thus be optimized, for example, with regard to band width, modulation range or load capacity. The filter circuit according to the invention further has the advantage that no voltage build-up occurs within the filter configuration, as a result of which comparatively large signals can still be processed without being distorted. In fact, in contrast with the known filter circuits of higher order, there are now no amplifier outputs, such as, for example, those of the amplifier 20 in the circuit of Fig. 1, which can convey uncontrolled high signal voltages due to resonance.

The transfer function of a filter can be written as:

$$\frac{U_{out}}{U_{in}} = \frac{N(P)}{D(P)} = \frac{N'(P) * \text{PRODUCT}_K(P + Z_K) * \text{PRODUCT}_K(P + C_K)}{D'(P) * \text{PRODUCT}_K(P + P_K) * \text{PRODUCT}_K(P + C_K)} \quad (2)$$

There are separated out of $N(P)$ nN_r separate negative real zero points and out of $D(P)$ nD_r separate negative real zero points. If the degrees of the polynomials $N(P)$ and $D(P)$ are set to nN and nD , respectively, the degree of $N'(P)$ is equal to $nN - nN_r$ and that of $D'(P)$ is equal to $nD - nD_r$. A number n_c of the negative real zero points in $N(P)$ and $D(P)$ are additional common factors $P + C_K$. The equation (2) can be rewritten as:

$$\frac{N(P)}{D(P)} = \frac{N'(P)}{\text{PRODUCT}_K(P + P_K) * \text{PRODUCT}_K(P + C_K)} \cdot \frac{D'(P)}{\text{PRODUCT}_K(P + Z_K) * \text{PRODUCT}_K(P + C_K)} = Y_N(P) / Y_D(P) \quad (3)$$

The terms $Y_N(P)$ and $Y_D(P)$ are each a quotient of polynomials in P . When it is ensured that all poles of $Y_N(P)$ and of $Y_D(P)$ are different and lie on the negative real axis, $Y_N(P)$ and $Y_D(P)$ can be constructed as admittances, which are connected in the manner shown in Fig. 2a. In this Figure, a balanced filter circuit is shown having filter inputs 1, 2, which are connected via an admittance $Y_N(P)$ to the non-inverting input 5 and the inverting input 6 of a balanced amplifier 10, whose inverting output 7 and whose non-inverting output 8 are connected via an admittance $Y_D(P)$ to the non-inverting input 5 and the inverting input 6, respectively, and further directly to the filter outputs 3 and 4, respectively. For the circuit of Fig. 2a the relation (3) holds.

For the degrees of the numerator and the denominator of the admittances $Y_N(P)$ and $Y_D(P)$ it holds that:

Numerator $Y_N(P)$: $nN - nN_r$

denominator $Y_N(P)$: $nD_r + n_c$

numerator $Y_D(P)$: $nD - nD_r$

denominator $Y_D(P)$: $nN_r + n_c$.

The actions:

- 1) release of a factor $P + Z_K$ from $N(P)$
- 2) release of a factor $P + P_K$ from $D(P)$ and
- 3) take-up of a common factor $P + C_K$,

result in that the degree of the numerator minus the degree of the denominator of $Y_N(P)$ and of $Y_D(P)$ decreases per action by one. The actions 1), 2) and 3) are repeated until the degree of the numerator minus the degree of the denominator of $Y_N(P)$ and of $Y_D(P)$ has fallen to one or lower, in general a minimum number of common

factors $P+C_K$ being taken up in order that the complexity of the resulting filter circuit is not unnecessarily enlarged.

The result is a transfer function $N(P)/D(P) = Y_N(P)/Y_D(P)$, in which for $Y_N(P)$ and $Y_D(P)$ it holds that:

- they are quotients of polynomes with real coefficients,
- all poles are different and are located on the negative real axis

and

- the degree of the numerator is at most 1 higher than the degree of the denominator.

$Y_N(P)$ and $Y_D(P)$ can now be written by breaking into partial fractions as:

$$Y_N(P), Y_D(P) = a + b \cdot P + \sum_k (P \cdot A_k / (P + B_k)) \quad (6)$$

In which a , b , A_k and B_k are real and B_k is positive. The term a is the conduction of a resistor having a value $1/a$. The term $b \cdot P$ is the admittance of a capacitor having a value b . The term $P \cdot A_k / (P + B_k)$ is the admittance of a series-combination of a resistor having a value $1/A_k$ and a capacitor having a value A_k/B_k . Negative values of a , b and A_k are discounted by cross-coupling of the relevant admittances, as shown in Figs. 2b and 2c. In these Figures, corresponding parts have the same reference numerals as in Fig. 2a. Fig. 2b indicates how a pair of admittances Y_1 is cross-coupled between the filter inputs 1, 2 and the inputs 5, 6 of the amplifier 10. One admittance of the pair of admittances is connected between the filter input 1 and the inverting input 6 and the other admittance is connected between the filter input 2 and the non-inverting input 5. In Fig. 2c, one admittance of the pair of admittances Y_4 is connected between the inverting output 7 and the inverting input 6 and the other admittance is connected between the non-inverting output 8 and the non-inverting input 5. Fig. 2d shows a balanced amplifier, which is provided not only with cross-couplings with pairs of admittances Y_1 and Y_4 , as indicated in Figs. 2b and 2c, but is also provided in the manner indicated for $Y_N(P)$ and $Y_D(P)$ in Fig. 2a with pairs of admittances Y_2 and Y_3 , respectively. For the transfer function of the circuit of Fig. 2d there can now be written:

$$\frac{U_{out}}{U_{in}} = \frac{Y_N(P)}{Y_D(P)} = \frac{Y_1(P) - Y_2(P)}{Y_3(P) - Y_4(P)} \quad (7)$$

Positive terms in the equation (6) together form the admittances $Y_1(P)$ or $Y_3(P)$, while negative terms are united in the admittances $Y_2(P)$ or $Y_4(P)$.

With reference to a few examples, the design of N^{th} order filter circuits ($N \geq 2$) comprising one balanced amplifier will now be described. In these examples, the transfer functions H_N can be multiplied by the amplification factor M in order that a given amplification or attenuation from the input signal to the output signal of the filter circuit is obtained. This factor M can be simply attained in that either the admittances Y_1 and Y_2 or the admittances Y_3 and Y_4 are multiplied by a factor M . This means that of the relevant admittance the values of resistors must be divided by M and the values of capacitors must be multiplied by M .

Example 1: second order resonance circuit.

The transfer function thereof is:

$$\frac{U_{out}}{U_{in}} = \frac{Y_N(P)}{Y_D(P)} = \frac{P \cdot W_0/Q_0}{P \cdot P + P \cdot W_0/Q_0 + W_0 \cdot W_0} \quad (8)$$

Therein, W_0 is the resonance frequency and Q_0 is the Q factor, for which it is assumed that $Q_0 > 1/2$. The poles are additively complex. For $Y_N(P)$ and $Y_D(P)$, the common factor $(P+a)$ is introduced:

$$Y_N(P) = \frac{W_0}{Q_0} \cdot \frac{P}{P+a} \quad (9A)$$

$$Y_D(P) = \frac{P \cdot P + P \cdot W_0/Q_0 + W_0 \cdot W_0}{P+a} = \quad (9B)$$

$$= AA + BB \cdot P + A \cdot P/(P+a) \quad (9C)$$

in which:

$$AA = W_0 \cdot W_0/a$$

$$BB = 1$$

$$A = -a + W_0/Q_0 - W_0 \cdot W_0/a < 0$$

The coefficient A is negative, for in:

$$A = -W_0 \left(\frac{a}{W_0} + \frac{W_0}{a} - \frac{1}{Q_0} \right)$$

is

$$\frac{a}{W_0} + \frac{W_0}{a} \geq 2, \text{ while } \frac{1}{Q_0} < 2$$

YN(P) is a positive admittance of an RC series-combination in the position of Y2 in the circuit of Fig. 2d. YD(P) consists of the positive admittances AA and BB*P, which must be arranged in the position Y4. In this example, there is no admittance Y1, i.e. Y1(P) = 0. The result is shown in the filter circuit of Fig. 3, in which corresponding parts have the same reference numerals as in Fig. 2. The admittances of the second pair of admittances Y2 are constituted by a series-combination of a resistor R1 and a capacitor C1, those of the third pair of admittances Y3 by a parallel-combination of a resistor R2 and a capacitor C2 and those of the fourth pair of admittances by a series-combination of a resistor R3 and a capacitor C3, where:

$$R1 = Q_0/W_0$$

$$C1 = W_0/(Q_0 \cdot a)$$

$$R2 = a/(W_0 \cdot W_0)$$

$$C2 = 1$$

$$R3 = -1/A$$

$$C3 = -A/a$$

All resistor values may be multiplied by a given scale factor if at the same time all capacitor values are divided by the same scale factor. The quotient YN(P)/YD(P) consequently does not change in the transfer function Uout/Uin of the filter circuit.

The value of a can be freely chosen. The choice $a = W_0$ now yields substitution in the equation (9A) and (9C):

$$Y_N(P) = \frac{W_0}{Q_0} * \frac{P}{P + W_0} \quad (10A)$$

$$Y_D(P) = W_0 + P + \left(\frac{W_0}{Q_0} - 2 W_0\right) * \frac{P}{P + W_0} \quad (10B)$$

The third term of YD(P) in the equation (10B) can be seen as the sum of a positive admittance and of a negative admittance, each consisting of a series-combination of a resistor and a capacitor.

In Fig. 4, in which corresponding parts have the same reference numerals as in Fig. 3, the resulting filter circuit is shown. The admittances Y2, Y3 and Y4 of Fig. 2d now correspond to the series-combination of a resistor R11 and a capacitor C11, to a parallel-combination of a resistor R12, a capacitor C12 and a series-combination of a resistor R13 and a capacitor C13 and to a series-combination of a resistor R14 and a capacitor C14, respectively. After multiplication of all resistor values by $W_0 \cdot R$ and with the assumption that $C = 1/(W_0 \cdot R)$ it follows for the values of the resistors and capacitors of the filter circuit of Fig. 4 that:

$$R11 = R13 = Q_0 \cdot R$$

$$C11 = C13 = C/Q_0$$

$$R12 = R$$

$$C12 = C$$

$$R14 = R/2$$

$$C14 = 2 \cdot C$$

$$R \cdot C = 1/W_0$$

This filter circuit is suitable for resonance circuits having not too high a Q_0 .

Example 2: second order all-pass filter.

In a first version, the poles are unequal and lie on the negative real axis. The transfer function can then be written as:

$$\frac{U_{out}}{U_{in}} = \frac{Y_N(P)}{Y_D(P)} = \frac{(P - a)(P - b)}{(P + a)(P + b)} \quad (11)$$

in which $a > b$.

On behalf of fraction splitting of YN(P) and YD(P), in this case no additional common factors are required. This otherwise also holds always for all-pass transfer functions with real poles of any order.

When choosing for

$$Y_N(P) = \frac{(P - a)(P - b)}{(P + a)(P + b)}$$

and for YD(P) = 1, after fraction splitting there is obtained:

$$Y_N(P) = 1 + A * P/(P + a) + B * P/(P + b) \quad (12A)$$

$$Y_D(P) = 1 \quad (12B)$$

In which

$$A = 2 * (a + b) / (a - b) > 0$$

and

$$B = -2 * (a + b) / (a - b) < 0$$

YN(P) consists of the sum of a positive admittance and a negative admittance so that the admittances Y1 and Y2 in the circuit of Fig. 2d now both have a value unequal to zero. YD(P) consists only of a positive admittance so that the admittance Y4 is now absent in the circuit and only the admittance Y3 is present. Fig. 5 shows the resulting filter circuit. Corresponding parts have the same reference numerals as in Fig. 4. The admittance Y1 is now a parallel-combination of a resistor R21 and a series-combination of a resistor R22 and a capacitor C21. The admittance Y2 is a series-combination of a resistor R23 and a capacitor C22 and the admittance Y3 consists of a resistor R24. It follows from (12A) and (12B) that:

$$R21 = R24 = 1$$

$$R22 = R23 = 1/A$$

$$C21 = C22 = A/a.$$

Also in this case, the resistor values and capacitor values may be scaled as indicated in Example 1.

In a second version of a second order all-pass filter, the poles are complex:

$$\frac{U_{out}}{U_{in}} = \frac{P * P - P * W_o/Q_o + W_o * W_o}{P * P + P * W_o/Q_o + W_o * W_o} = \frac{Y_N(P)}{Y_D(P)} \quad (13)$$

in which $Q_o \geq 1/2$.

For YN(P) and YD(P), a common factor (P+c) is introduced. Partial fraction splitting then yields:

$$Y_N(P) = (P * P - P * W_o/Q_o + W_o * W_o) / (P + c) \\ = W_o * W_o / c + P + A * P / (P + c) \quad (14A)$$

$$Y_D(P) = (P * P + P * W_o/Q_o + W_o * W_o) / (P + c) \\ = W_o * W_o / c + P + B * P / (P + c) \quad (14B)$$

In which:

$$A = -c - W_o/Q_o - W_o * W_o / c < 0$$

$$B = -c + W_o/Q_o - W_o * W_o / c < 0$$

The factors A and B are both negative. c can still be chosen freely. For $c = W_o$ and with $R * C = 1/W_o$, the circuit of Fig. 6 is obtained, in which corresponding parts have the same reference numerals as in Fig. 5. Both YN(P) and YD(P) now comprise positive and negative admittances so that all admittances Y1, Y2, Y3 and Y4 of the circuit of Fig. 2d have a value unequal to zero. The admittance Y1 is a parallel-combination of a resistor R31 and a capacitor C31. The admittance Y2 is a parallel-combination of a first series-combination of a resistor R32 and a capacitor C32, and a second series-combination of a resistor R33 and a capacitor C33. The admittance Y3 is composed of a parallel-combination of a resistor R34, a capacitor C34 and the series-combination of a resistor R35 and a capacitor C35. The admittance Y4 is a series-combination of a resistor R36 and a capacitor C36. For the values of the resistors and capacitors it holds that:

$$R31 = R34 = R$$

$$C31 = C34 = C$$

$$R32 = R35 = R/2$$

$$C32 = C35 = 2 * C$$

$$R33 = R36 = Q_o * R$$

$$C33 = C36 = C/Q_o$$

$$R * C = 1/W_o$$

If further Q_o is chosen to be equal to 1/2 (equal real poles in the transfer function), the resistors R32 and R33 and the capacitors C32 and C33 are equal to each other. The admittance Y2 can then be replaced by one series-combination of a resistor and a capacitor.

Example 3: third order all-pass filter.

The transfer function is:

$$\frac{U_{out}}{U_{in}} = \frac{Y_N(P)}{Y_D(P)} = \frac{(P * P - a * P + b) * (P - c)}{(P * P + a * P + b) * (P + c)} \quad (15)$$

with $a, b, c > 0$.

It is assumed that the transfer function has a complex polepair so that: $a * a < 4 * b$. On behalf of partial fraction splitting, the numerator and the denominator of the righthand term in the equation (15) are divided by (P+c).

Further, the common factor $(P+d)$ is introduced, where $d > 0$, and $\underline{d}$ is unequal to $\underline{c}$. As a result, $Y_N(P)$ and $Y_D(P)$ can be written as:

$$Y_N(P) = \frac{(P * P - a * P + b) * (P - c)}{(P + c) * (P + d)} \\ = -b/d + P + A * P/(P + c) + B * P/(P + d) \quad (16A)$$

$$Y_D(P) = \frac{P * P + a * P + b}{P + d} = b/d + P + C * P/(P + d) \quad (16B)$$

in which

$$A = 2 * (c * c + a * c + b)/(d - c)$$

$$B = -(d + a + b/d) * (d + c)/(d - c)$$

$$C = -(d - a + b/d)$$

Since $a * a < 4 * b$, $C < 0$. If now $\underline{d}$ is chosen to be larger than $\underline{c}$, $A > 0$ and $B < 0$. The sign of the component admittances is determined thereby and the implementation thereof is indicated in the filter circuit of Fig. 7, in which corresponding parts have the same reference numerals as in Fig. 6. The admittances Y_1 , Y_2 , Y_3 and Y_4 of Fig. 2d are composed as follows: Y_1 is a parallel-combination of a capacitor C_{41} and a series-combination of a resistor R_{41} and a capacitor C_{42} ; Y_2 is a parallel-combination of a resistor R_{42} and a series-combination of a resistor R_{43} and a capacitor C_{43} ; Y_3 is a parallel-combination of a resistor R_{44} and a capacitor C_{44} ; Y_4 is a series-combination of a resistor R_{45} and a capacitor C_{45} . For the values of the resistors and capacitors, it holds that:

$$C_{41} = 1$$

$$R_{41} = 1/A$$

$$C_{42} = A/c$$

$$R_{42} = b/d$$

$$R_{43} = -1/B$$

$$C_{43} = -B/d$$

$$R_{44} = b/d$$

$$C_{44} = 1$$

$$R_{45} = -1/C$$

$$C_{45} = -C/d$$

The values of the resistors and capacitors in this case may also be scaled again as indicated in Example 1. The filter circuit of Fig. 7 may be used, for example, as a delay section having a bandwidth $\underline{b}$ Hz and a delay $\underline{d}$ seconds, in which $b * d = 1/2$. The delay $d = 1/(2 * b)$ is then equal to the time interval between two samples of a signal sampled according to Nyquist with $2b$ Hz and having a bandwidth $\underline{b}$.

As appears from the Figures, the admittances Y_1 , Y_2 , Y_3 and/or Y_4 may be of fairly complicated nature. With increasing order of the filter circuit it may be advantageous to replace one or more of the admittances Y_1 , Y_2 , Y_3 , Y_4 by an equivalent RC ladder type network having an admittance Y_K ($K = 1, 2, 3$ or 4), as indicated in Fig. 8. The circuits shown in Figs. 8a, 8b, 8c and 8d can all represent with suitably chosen element values the same admittance Y_K . The construction of Fig. 8a is known as the Foster type, that of Figures 8b and 8c as the Cauer or ladder type, while Fig. 8d shows a mixed form.

An RC line can be approximately represented as an RC ladder, as shown in Fig. 9. Conversely, the admittance of an RC ladder can be approximated and implemented by means of an RC line. Therefore, it is possible to implement the pairs of admittances Y_1 , Y_2 , Y_3 and Y_4 fully or in part as RC lines, which may be advantageous especially with high frequencies. Other equivalent networks, such as non-uniformly distributed RC networks, as the case may be in combination with resistors and/or capacitors, are also possible.

The invention is not limited to the filter circuits of the embodiments described with the associated Figures. For any linear transfer function of any order, it is possible in a manner analogous to that described in the embodiments to determine the admittances Y_1 , Y_2 , Y_3 and Y_4 of the general filter circuit of Fig. 2d.

Claims

1. A balanced filter circuit having an Nth order transfer function H_N from a balanced input signal to a balanced output signal, N being an integer larger than or equal to two, comprising:
 - a first and a second filter input for supplying the balanced input signal;
 - a first and a second filter output for deriving the balanced output signal;
 - only one balanced amplifier having an inverting input and a non-inverting input and an inverting out-



Further, the common factor $(P+d)$ is introduced, where $d > 0$, and d is unequal to c . As a result, $Y_N(P)$ and $Y_D(P)$ can be written as:

$$Y_N(P) = \frac{(P^2 - aP + b)(P - c)}{(P + c)(P + d)}$$

$$= -b/d + P + A * P/(P + c) + B * P/(P + d) \quad (16A)$$

$$Y_D(P) = \frac{P^2 + aP + b}{P + d} = b/d + P + C * P/(P + d) \quad (16B)$$

In which

$$A = 2 * (c * c + a * c + b)/(d - c)$$

$$B = -(d + a + b/d) * (d + c)/(d - c)$$

$$C = -(d - a + b/d)$$

Since $a^2 < 4b$, $C < 0$. If now d is chosen to be larger than c , $A > 0$ and $B < 0$. The sign of the component admittances is determined thereby and the implementation thereof is indicated in the filter circuit of Fig. 7, in which corresponding parts have the same reference numerals as in Fig. 6. The admittances Y_1 , Y_2 , Y_3 and Y_4 of Fig. 2d are composed as follows: Y_1 is a parallel-combination of a capacitor C_{41} and a series-combination of a resistor R_{41} and a capacitor C_{42} ; Y_2 is a parallel-combination of a resistor R_{42} and a series-combination of a resistor R_{43} and a capacitor C_{43} ; Y_3 is a parallel-combination of a resistor R_{44} and a capacitor C_{44} ; Y_4 is a series-combination of a resistor R_{45} and a capacitor C_{45} . For the values of the resistors and capacitors, it holds that:

$$C_{41} = 1$$

$$R_{41} = 1/A$$

$$C_{42} = A/c$$

$$R_{42} = b/d$$

$$R_{43} = -1/B$$

$$C_{43} = -B/d$$

$$R_{44} = b/d$$

$$C_{44} = 1$$

$$R_{45} = -1/C$$

$$C_{45} = -C/d$$

The values of the resistors and capacitors in this case may also be scaled again as indicated in Example 1. The filter circuit of Fig. 7 may be used, for example, as a delay section having a bandwidth b Hz and a delay d seconds, in which $b \cdot d = 1/2$. The delay $d = 1/(2 \cdot b)$ is then equal to the time interval between two samples of a signal sampled according to Nyquist with $2b$ Hz and having a bandwidth b .

As appears from the Figures, the admittances Y_1 , Y_2 , Y_3 and/or Y_4 may be of fairly complicated nature. With increasing order of the filter circuit it may be advantageous to replace one or more of the admittances Y_1 , Y_2 , Y_3 , Y_4 by an equivalent RC ladder type network having an admittance Y_K ($K = 1, 2, 3$ or 4), as indicated in Fig. 8. The circuits shown in Figs. 8a, 8b, 8c and 8d can all represent with suitably chosen element values the same admittance Y_K . The construction of Fig. 8a is known as the Foster type, that of Figures 8b and 8c as the Caue or ladder type, while Fig. 8d shows a mixed form.

An RC line can be approximately represented as an RC ladder, as shown in Fig. 9. Conversely, the admittance of an RC ladder can be approximated and implemented by means of an RC line. Therefore, it is possible to implement the pairs of admittances Y_1 , Y_2 , Y_3 and Y_4 fully or in part as RC lines, which may be advantageous especially with high frequencies. Other equivalent networks, such as non-uniformly distributed RC networks, as the case may be in combination with resistors and/or capacitors, are also possible.

The invention is not limited to the filter circuits of the embodiments described with the associated Figures. For any linear transfer function of any order, it is possible in a manner analogous to that described in the embodiments to determine the admittances Y_1 , Y_2 , Y_3 and Y_4 of the general filter circuit of Fig. 2d.

Claims

1. A balanced filter circuit having an N th order transfer function H_N from a balanced input signal to a balanced output signal, N being an integer larger than or equal to two, comprising:
 - a first and a second filter input for supplying the balanced input signal;
 - a first and a second filter output for deriving the balanced output signal;
 - only one balanced amplifier having an inverting input and a non-inverting input and an inverting out-



put coupled to the first filter output and a non-inverting output coupled to the second filter output;
 - at least one of a first, second, third and fourth pair of admittances of a first and a second admittance, the first admittance of the first pair of admittances being connected between the first filter input and the inverting input and the second admittance being connected between the second filter input and the non-inverting input, the first admittance of the second pair of admittances being connected between the first filter input and the non-inverting input and the second admittance being connected between the second filter input and the inverting input, the first admittance of the third pair of admittances being connected between the inverting output and the non-inverting input and the second admittance being connected between the non-inverting output and the inverting input and the first admittance of the fourth pair of admittances being connected between the inverting output and the inverting input and the second admittance being connected between the non-inverting output and the non-inverting input.

2. A balanced filter circuit as claimed in Claim 1, characterized in that the filter circuit has a second order transfer function having the shape:

$$H_2 = \frac{M * P * W_o / Q_o}{P * P + P * W_o / Q_o + W_o * W_o}$$

in which

P = complex frequency,
 W_o = resonance frequency,
 Q_o = Q factor and Q_o > 1/2,
 M = amplification factor,

and

- the first and the second admittance of the second pair of admittances each comprise a series-combination of a first resistor having a value substantially equal to $K * Q_o / W_o / M$ and a first capacitor having a value substantially equal to $M * W_o / (Q_o * a * K)$;
- the first and the second admittance of the third pair of admittances each comprise a parallel-combination of a second resistor having a value substantially equal to $K * a / (W_o * W_o)$ and a capacitor having a value substantially equal to $1/K$;
- the first and the second admittance of the fourth pair of admittances each comprise a series-combination of a third resistor having a value substantially equal to $-K / (-a + W_o / Q_o - W_o * W_o)$ and a third capacitor having a value substantially equal to $-(-a + W_o / Q_o - W_o * W_o) / (a * K)$,

a and K being positive real numbers.

3. A balanced filter circuit as claimed in Claim 1, characterized in that the filter circuit has a second order transfer function having the shape:

$$H_2 = \frac{M * P * W_o / Q_o}{P * P + P * W_o / Q_o + W_o * W_o}$$

in which

P = complex frequency,
 W_o = resonance frequency,
 Q_o = Q factor and Q_o > 1/2,
 M = amplification factor,

and

- the first and the second admittance of the second pair of admittances each comprise the series-combination of a first resistor having a value substantially equal to $Q_o * R / M$ and a first capacitor having a value substantially equal to $M * C / Q_o$;
- the first and the second admittance of the third pair of admittances each comprise the parallel-combination of a second resistor having a value substantially equal to R, a second capacitor having a value substantially equal to C and a series-combination of a third resistor having a value substantially equal to $Q_o * R$ and a third capacitor having a value substantially equal to C / Q_o ;
- the first and the second admittance of the fourth pair of admittances each comprise a series-combination of a fourth resistor having a value substantially equal to $R/2$ and a fourth capacitor having a value substantially equal to $2 * C$;

R and C being constants to be chosen, for which it holds that

$$R * C = 1 / W_o.$$

4. A balanced filter circuit as claimed in Claim 1, characterized in that the filter circuit has a second order transfer function having the shape:



$$H_2 = \frac{M * (P - a)(P - b)}{(P + a)(P + b)}$$

in which

P = complex frequency,
 $a, b,$ = positive real number and $a > b$,
 M = amplification factor,

and

- the first and the second admittance of the first pair of admittances each comprise a parallel-combination of a first resistor having a value substantially equal to K/M and a series-combination of a second resistor having a value substantially equal to $K/M * (a-b)/(2 * (a+b))$ and a first capacitor having a value substantially equal to $2 * M(a+b)/(K * a * (a-b))$;
- the first and the second admittance of the second pair of admittances each comprise a series-combination of a third resistor having a value substantially equal to that of a second resistor and a second capacitor having a value substantially equal to that of the first capacitor;
- the first and the second admittance of the third pair of admittances each comprise a fourth resistor having a value substantially equal to that of the first resistor, K being a positive real number.

5. A balanced filter circuit as claimed in Claim 1, characterized in that the filter circuit has a second order transfer function having the shape:

$$H_2 = \frac{P * P - P * W_0/Q_0 + W_0 * W_0}{P * P + P * W_0/Q_0 + W_0 * W_0} * M$$

in which

P = complex frequency,
 W_0 = resonance frequency,
 Q_0 = Q factor and $Q_0 \geq 1/2$,
 M = amplification factor,

and

- the first and the second admittance of the first pair of admittances each comprise a parallel-combination of a first resistor having a value substantially equal to R/M and a first capacitor having a value substantially equal to $M * C$;
- the first and the second admittance of the second pair of admittances each comprise a parallel-combination of a series-combination of a second resistor having a value substantially equal to $R/(2 * M)$ and a second capacitor having a value substantially equal to $2 * M * C$ and a series-combination of a third resistor having a value substantially equal to $Q_0 * R/M$ and a third capacitor having a value substantially equal to $M * C/Q_0$;
- the first and the second admittance of the third pair of admittances each comprise a parallel-combination of a fourth resistor having a value substantially equal to R , a fourth capacitor having a value substantially equal to C and a series-combination of a fifth resistor having a value substantially equal to $R/2$ and a fifth capacitor having a value substantially equal to $2 * C$;
- the first and the second admittance of the fourth pair of admittances each comprise a series-combination of a sixth resistor having a value substantially equal to $Q_0 * R$ and a sixth capacitor having a value substantially equal to C/Q_0 ,

R and C being constants to be chosen, for which it holds that:

$$R * C = 1/W_0.$$

6. A balanced filter circuit as claimed in Claim 1, characterized in that the filter circuit has a third order transfer function having the shape:

$$H_3 = \frac{(P * P - a * P + b)(P - c)}{(P * P + a * P + b)(P + c)} * M$$

in which

P = complex frequency,
 a, b, c = a real positive number larger than zero and $a * a < 4 * b$
 M = amplification factor

and

- the first and the second admittance of the first pair of admittances each comprise a parallel-combination of a first capacitor having a value substantially equal to M/K and the series-combination of a first resistor having a value substantially equal to $K/A/M$ and a second capacitor having a value substantially equal to $M * A/(c * K)$



- the first and the second admittance of the second pair of admittances each comprise a parallel-combination of a second resistor having a value substantially equal to $K/M \cdot b/d$ and a series-combination of a third resistor having a value substantially equal to $-K/B/M$ and a third capacitor having a value substantially equal to $-B \cdot M/(d \cdot K)$;
- 5 - the first and the second admittance of the third pair of admittances each comprise a parallel-combination of a fourth resistor having a value substantially equal to $K \cdot b/d$ and a capacitor having a value substantially equal to $1/K$;
- the first and the second admittance of the fourth pair of admittances each comprise a series-combination of a fifth resistor having a value substantially equal to $-K/C$ and a fifth capacitor having a value substantially equal to $-C/(d \cdot K)$,

10 d being a positive real number larger than c ,

$$A = 2 \cdot (c \cdot c + a \cdot c + b)/(d - c),$$

$$B = -(d + a + b/d)(d + c)/(d - c),$$

$$C = -(d - a + b/d),$$

15 and K being a positive real number.

7. A balanced filter circuit as claimed in any one of the preceding Claims, characterized in that at least one of the said admittances is composed of an equivalent RC network having substantially the same admittance.

Patentansprüche

1. Gegentakt-Filterschaltung mit einer Übertragungsfunktion H_N N-ter Ordnung von einem Gegentakt-Eingangssignal in ein Gegentakt-Ausgangssignal, wobei N eine ganze Zahl größer oder gleich zwei ist, mit:
- einem ersten und einem zweiten Filtereingang zum Zuführen eines Gegentakt-Eingangssignals;
 - einem ersten und einem zweiten Filterausgang zum Abnehmen des Gegentakt-Ausgangssignals;
 - nur einem Gegentaktverstärker mit einem invertierenden Eingang und einem nichtinvertierenden Eingang und einem mit dem ersten Filterausgang gekoppelten invertierenden Ausgang und einen mit dem zweiten Filterausgang gekoppelten nichtinvertierenden Ausgang;
 - mindestens einem ersten, zweiten, dritten und vierten Admittanzpaar aus einer ersten und einer zweiten Admittanz,

wobei die erste Admittanz des ersten Admittanzpaares zwischen den ersten Filtereingang und den invertierenden Eingang und die zweite Admittanz zwischen den zweiten Filtereingang und den nichtinvertierenden Eingang geschaltet ist, die erste Admittanz des zweiten Admittanzpaares zwischen den ersten Filtereingang und den nichtinvertierenden Eingang und die zweite Admittanz zwischen den zweiten Filtereingang und den invertierenden Eingang geschaltet ist, die erste Admittanz des dritten Admittanzpaares zwischen den invertierenden Ausgang und den nichtinvertierenden Eingang und die zweite Admittanz zwischen den nichtinvertierenden Ausgang und den invertierenden Eingang geschaltet ist und die erste Admittanz des vierten Admittanzpaares zwischen den ersten invertierenden Ausgang und den invertierenden Eingang und die zweite Admittanz zwischen den nichtinvertierenden Ausgang und den nichtinvertierenden Eingang geschaltet ist.

2. Gegentakt-Filterschaltung nach Anspruch 1, dadurch gekennzeichnet, daß die Filterschaltung eine Übertragungsfunktion zweiter Ordnung hat, mit der Form:

$$H_2 = \frac{M \cdot P W_0 / Q_0}{p \cdot p + p \cdot W_0 / Q_0 + W_0 \cdot W_0}$$

mit

P = komplexe Frequenz,

W_0 = Resonanzfrequenz,

Q_0 = Q-Faktor und $Q_0 > 1/2$,

M = Verstärkungsfaktor,

und

- die erste und die zweite Admittanz des zweiten Admittanzpaares jeweils eine Reihenschaltung aus einem ersten Widerstand mit einem Wert nahezu gleich $K \cdot Q_0 / W_0 / M$ und einem ersten Kondensator mit einem Wert nahezu gleich $M \cdot W_0 / (Q_0 \cdot a \cdot K)$ umfassen;
- die erste und die zweite Admittanz des dritten Admittanzpaares jeweils eine Parallelschaltung aus einem zweiten Widerstand mit einem Wert nahezu gleich $K \cdot a / (W_0 \cdot W_0)$ und einem Kondensator mit



einem Wert nahezu gleich $1/K$ umfassen;

- die erste und die zweite Admittanz des vierten Admittanzpaares jeweils eine Reihenschaltung aus einem dritten Widerstand mit einem Wert nahezu gleich $-K/(-a+Wo/Qo-Wo*Wo)$ und einem dritten Kondensator mit einem Wert nahezu gleich $-(a + Wo/Qo-Wo*Wo)/(a*K)$ umfassen,

wobei a und K positive reelle Zahlen sind.

3. Gegentakt-Filterschaltung nach Anspruch 1, dadurch gekennzeichnet, daß die Filterschaltung eine Übertragungsfunktion zweiter Ordnung hat, mit der Form:

$$H_2 = \frac{M * P W_o / Q_o}{p * p + p * W_o / Q_o + W_o * W_o}$$

mit

P = komplexe Frequenz,

W_o = Resonanzfrequenz,

Q_o = Q-Faktor und $Q_o > 1/2$,

M = Verstärkungsfaktor,

und

- die erste und die zweite Admittanz des zweiten Admittanzpaares jeweils eine Reihenschaltung aus einem ersten Widerstand mit einem Wert nahezu gleich $Q_o * R / M$ und einem ersten Kondensator mit einem Wert nahezu gleich $M * C / Q_o$ umfassen;
- die erste und die zweite Admittanz des dritten Admittanzpaares jeweils eine Parallelschaltung aus einem zweiten Widerstand mit einem Wert nahezu gleich R , einem zweiten Kondensator mit einem Wert nahezu gleich C und einer Reihenschaltung aus einem dritten Widerstand mit einem Wert nahezu gleich $Q_o * R$ und einem dritten Kondensator mit einem Wert nahezu gleich C / Q_o umfassen;
- die erste und die zweite Admittanz des vierten Admittanzpaares jeweils eine Reihenschaltung aus einem vierten Widerstand mit einem Wert nahezu gleich $R/2$ und einem vierten Kondensator mit einem Wert nahezu gleich $2 * C$ umfassen;

mit R und C zu wählende Konstanten, für die gilt:

$$R * C = 1 / W_o.$$

4. Gegentakt-Filterschaltung nach Anspruch 1, dadurch gekennzeichnet, daß die Filterschaltung eine Übertragungsfunktion zweiter Ordnung hat, mit der Form:

$$H_2 = \frac{M * (P - a)(P - b)}{(P + a)(P + b)}$$

mit

P = komplexe Frequenz,

a, b = positive reelle Zahl und $a > b$,

M = Verstärkungsfaktor,

und

- die erste und die zweite Admittanz des ersten Admittanzpaares jeweils eine Parallelschaltung aus einem ersten Widerstand mit einem Wert nahezu gleich K/M und einer Reihenschaltung aus einem zweiten Widerstand mit einem Wert nahezu gleich $KM * (a-b)/(2 * (a+b))$ und einem ersten Kondensator mit einem Wert nahezu gleich $2 * M(a+b)/(K * a * (a-b))$ umfassen;
- die erste und die zweite Admittanz des zweiten Admittanzpaares jeweils eine Reihenschaltung aus einem dritten Widerstand mit einem Wert nahezu gleich dem eines zweiten Widerstandes und einem zweiten Kondensators mit einem Wert nahezu gleich dem des ersten Kondensators umfassen;
- die erste und die zweite Admittanz des dritten Admittanzpaares jeweils einen vierten Widerstand mit einem Wert nahezu gleich dem des ersten Widerstandes umfassen, wobei K eine positive reelle Zahl ist.

5. Gegentakt-Filterschaltung nach Anspruch 1, dadurch gekennzeichnet, daß die Filterschaltung eine Übertragungsfunktion zweiter Ordnung hat, mit der Form:

$$H_2 = \frac{P * P - P * W_o / Q_o + W_o * W_o}{P * P + P * W_o / Q_o + W_o * W_o} * M$$

mit

P = komplexe Frequenz,

W_o = Resonanzfrequenz,

Q_o = Q-Faktor und $Q_o \geq 1/2$,

M = Verstärkungsfaktor,



und

- die erste und die zweite Admittanz des zweiten Admittanzpaares jeweils eine Parallelschaltung aus einem ersten Widerstand mit einem Wert nahezu gleich R/M und einem ersten Kondensator mit einem Wert nahezu gleich $M \cdot C$ umfassen;
- die erste und die zweite Admittanz des zweiten Admittanzpaares jeweils eine Parallelschaltung aus einer Reihenschaltung aus einem zweiten Widerstand mit einem Wert nahezu gleich $R/2 \cdot M$ und einem zweiten Kondensator mit einem Wert nahezu gleich $2 \cdot M \cdot C$ und einer Reihenschaltung aus einem dritten Widerstand mit einem Wert nahezu gleich $Q_0 \cdot R/M$ und einem dritten Kondensator mit einem Wert nahezu gleich $M \cdot C/Q_0$ umfassen;
- die erste und die zweite Admittanz des dritten Admittanzpaares jeweils eine Parallelschaltung aus einem vierten Widerstand mit einem Wert nahezu gleich R , einem vierten Kondensator mit einem Wert nahezu gleich C und einer Reihenschaltung aus einem fünften Widerstand mit einem Wert nahezu gleich $R/2$ und einem fünften Kondensator mit einem Wert nahezu gleich $2 \cdot C$ umfassen;
- die erste und die zweite Admittanz des vierten Admittanzpaares jeweils eine Reihenschaltung aus einem sechsten Widerstand mit einem Wert nahezu gleich $Q_0 \cdot R$ und einem sechsten Kondensator mit einem Wert nahezu gleich C/Q_0 umfassen;

mit R und C zu wählende Konstanten, für die gilt

$$R \cdot C = 1/W_0.$$

6. Gegentakt-Filterschaltung nach Anspruch 1, dadurch gekennzeichnet, daß die Filterschaltung eine Übertragungsfunktion dritter Ordnung hat, mit der Form:

$$H_3 = \frac{(P \cdot P - a \cdot P + b)(P - c)}{(P \cdot P + a \cdot P + b)(P + c)} \cdot M$$

mit

- P = komplexe Frequenz,
 a, b, c = positive reelle Zahl größer als null und $a \cdot a < 4 \cdot b$,
 M = Verstärkungsfaktor,

und

- die erste und die zweite Admittanz des ersten Admittanzpaares jeweils eine Parallelschaltung aus einem ersten Kondensator mit einem Wert nahezu gleich M/K und der Reihenschaltung aus einem ersten Widerstand mit einem Wert nahezu gleich $K/A/M$ und einem zweiten Kondensator mit einem Wert nahezu gleich $M \cdot A/(c \cdot K)$ umfassen;
- die erste und die zweite Admittanz des zweiten Admittanzpaares jeweils eine Parallelschaltung aus einem zweiten Widerstand mit einem Wert nahezu gleich $K/M \cdot b/d$ und einer Reihenschaltung aus einem dritten Widerstand mit einem Wert nahezu gleich $-K/B/M$ und einem dritten Kondensator mit einem Wert nahezu gleich $-B \cdot M/(d \cdot K)$ umfassen;
- die erste und die zweite Admittanz des dritten Admittanzpaares jeweils eine Parallelschaltung aus einem vierten Widerstand mit einem Wert nahezu gleich $K \cdot b/d$ und einem Kondensator mit einem Wert nahezu gleich $1/K$ umfassen;
- die erste und die zweite Admittanz des vierten Admittanzpaares jeweils eine Reihenschaltung aus einem fünften Widerstand mit einem Wert nahezu gleich $-K/C$ und einem fünften Kondensator mit einem Wert nahezu gleich $-C/(d \cdot k)$ umfassen;

wobei d eine positive reelle Zahl größer als c ist,

$$A = 2 \cdot (c \cdot c + a \cdot c + b)/(d - c),$$

$$B = -(d + a + b/d)(d + c)/(d - c),$$

$$C = -(d - a + b/d)$$

und K eine positive reelle Zahl ist.

7. Gegentakt-Filterschaltung nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß mindestens eine der genannten Admittanzen aus einem äquivalenten RC-Netzwerk mit nahezu der gleichen Admittanz zusammengesetzt ist.

Revendications

1. Circuit de filtrage équilibré ayant une fonction de transfert H_N d'ordre N entre le signal d'entrée équilibré et le signal de sortie équilibré, N étant un entier supérieur ou égal à deux, comprenant :
- une première et une seconde entrée de filtre pour l'introduction du signal d'entrée équilibré;



- une première et une seconde sortie de filtre pour la dérivation du signal de sortie équilibré;
- un seul amplificateur équilibré ayant une entrée inversée et une entrée non inversée et une sortie inversée couplée à la première sortie de filtre et une sortie non inversée couplée à la seconde sortie de filtre;
- 5 - au moins une paire d'admittances d'une première, seconde, troisième et quatrième paire d'admittances d'une première et d'une seconde admittance,

la première admittance de la première paire d'admittances étant connectée entre la première entrée de filtre et l'entrée inversée et la seconde admittance étant connectée entre la seconde entrée de filtre et l'entrée non inversée, la première admittance de la seconde paire d'admittances étant connectée entre la première entrée de filtre et l'entrée non inversée et la seconde admittance étant connectée entre la seconde entrée de filtre et l'entrée inversée, la première admittance de la troisième paire d'admittances étant connectée entre la sortie inversée et l'entrée non inversée et la seconde admittance étant connectée entre la sortie non inversée et l'entrée inversée et la première admittance de la quatrième paire d'admittances étant connectée entre la sortie inversée et l'entrée inversée et la seconde admittance étant connectée entre la sortie non inversée et l'entrée non inversée.

2. Circuit de filtrage équilibré suivant la revendication 1, caractérisé en ce que le circuit de filtrage possède une fonction de transfert de second ordre de la forme : dans laquelle

P = fréquence complexe,

$$H_2 = \frac{M * P * W_0 / Q_0}{P * P + P * W_0 / Q_0 + W_0 * W_0}$$

W₀ = fréquence de résonance,

Q₀ = facteur Q et Q₀ > 1/2,

M = facteur d'amplification,

et

- la première et la seconde admittance de la seconde paire d'admittances comprennent chacune une combinaison en série d'une première résistance ayant une valeur pratiquement égale à $K * Q_0 / W_0 / M$ et d'un premier condensateur ayant une valeur pratiquement égale à $M * W_0 / (Q_0 * a * K)$;
- la première et la seconde admittance de la troisième paire d'admittances comprennent chacune une combinaison en parallèle d'une seconde résistance ayant une valeur pratiquement égale à $K * a / (W_0 * W_0)$ et d'un condensateur ayant une valeur pratiquement égale à $1/K$;
- la première et la seconde admittance de la quatrième paire d'admittances comprennent chacune une combinaison en série d'une troisième résistance ayant une valeur pratiquement égale à $-K / (-a + W_0 / Q_0 - W_0 * W_0)$ et d'un troisième condensateur ayant une valeur pratiquement égale à $-(-a + W_0 / Q_0 - W_0 * W_0) / (a * K)$,

a et K étant des nombres réels positifs.

3. Circuit de filtrage équilibré suivant la revendication 1, caractérisé en ce que le circuit de filtrage possède une fonction de transfert de second ordre de la forme :

$$H_2 = \frac{M * P * W_0 / Q_0}{P * P + P * W_0 / Q_0 + W_0 * W_0}$$

dans laquelle

P = fréquence complexe,

W₀ = fréquence de résonance,

Q₀ = facteur Q et Q₀ > 1/2,

M = facteur d'amplification,

et

- la première et la seconde admittance de la seconde paire d'admittances comprennent chacune la combinaison en série d'une première résistance ayant une valeur pratiquement égale à $Q_0 * R / M$ et d'un premier condensateur ayant une valeur pratiquement égale à $M * C / Q_0$;
- la première et la seconde admittance de la troisième paire d'admittances comprennent chacune la combinaison en parallèle d'une seconde résistance ayant une valeur pratiquement égale à R, d'un second condensateur ayant une valeur pratiquement égale à C et d'une combinaison en série d'une troisième résistance ayant une valeur pratiquement égale à $Q_0 * R$ et d'un troisième condensateur ayant une valeur pratiquement égale à C / Q_0 ;
- la première et la seconde admittance de la quatrième paire d'admittances comprennent chacune une combinaison en série d'une quatrième résistance ayant une valeur pratiquement égale à $R/2$ et d'un quatrième condensateur ayant une valeur pratiquement égale à $2 * C$,



R et C étant des constantes à choisir telles que :

$$R * C = 1/W_o.$$

4. Circuit de filtrage équilibré suivant la revendication 1, caractérisé en ce que le circuit de filtrage possède une fonction de transfert du second ordre de la forme :

$$H_2 = \frac{M * (P - a)(P - b)}{(P + a)(P + b)}$$

où

P = fréquence complexe,

a, b = nombre réel positif et a > b,

M = facteur d'amplification,

et

- la première et la seconde admittance de la première paire d'admittances comprennent chacune une combinaison en parallèle d'une première résistance ayant une valeur pratiquement égale à K/M et d'une combinaison en série d'une seconde résistance ayant une valeur pratiquement égale à K/M*(a-b)/[2*(a+b)] et d'un premier condensateur ayant une valeur pratiquement égale à 2*M(a+b)/[K*a*(a-b)];
- la première et la seconde admittance de la seconde paire d'admittances comprennent chacune une combinaison en série d'une troisième résistance ayant une valeur pratiquement égale à celle d'une seconde résistance et d'un second condensateur ayant une valeur pratiquement égale à celle du premier condensateur;
- la première et la seconde admittance de la troisième paire d'admittances comprennent chacune une quatrième résistance ayant une valeur pratiquement égale à celle de la première résistance, K étant un nombre réel positif.

5. Circuit de filtrage équilibré suivant la revendication 1, caractérisé en ce que le circuit de filtrage possède une fonction de transfert du second ordre de la forme :

$$H_2 = \frac{P * P - P * W_o/Q_o + W_o * W_o}{P * P + P * W_o/Q_o + W_o * W_o} * M$$

où

P = fréquence complexe,

W_o = fréquence de résonance,

Q_o = facteur Q ou Q_o ≥ 1/2,

M = facteur d'amplification,

et

- la première et la seconde admittance de la première paire d'admittances comprennent chacune une combinaison en parallèle d'une première résistance ayant une valeur pratiquement égale à R/M et d'un premier condensateur ayant une valeur pratiquement égale à M*C;
- la première et la seconde admittance de la seconde paire d'admittances comprennent chacune une combinaison en parallèle d'une combinaison en série d'une seconde résistance ayant une valeur pratiquement égale à R/(2*M) et d'un second condensateur ayant une valeur pratiquement égale à 2*M*C et d'une combinaison en série d'une troisième résistance ayant une valeur pratiquement égale à Q_o*R/M et d'un troisième condensateur ayant une valeur pratiquement égale à M*C/Q_o;
- la première et la seconde admittance de la troisième paire d'admittances comprennent chacune une combinaison en parallèle d'une quatrième résistance ayant une valeur pratiquement égale à R, d'un quatrième condensateur ayant une valeur pratiquement égale à C et d'une combinaison en série d'une cinquième résistance ayant une valeur pratiquement égale à R/2 et d'un cinquième condensateur ayant une valeur pratiquement égale à 2*C;
- la première et la seconde admittance de la quatrième paire d'admittances comprennent chacune une combinaison en série d'une sixième résistance ayant une valeur pratiquement égale à Q_o*R et d'un sixième condensateur ayant une valeur pratiquement égale à C/Q_o,

R et C étant des constantes à choisir telles que :

$$R * C = 1/W_o$$

6. Circuit de filtrage équilibré suivant la revendication 1, caractérisé en ce que le circuit de filtrage possède une fonction de transfert du troisième ordre de la forme :

$$H_3 = \frac{(P * P - a * P + b)(P - c)}{(P * P + a * P + b)(P - c)} * M$$



où

P = fréquence complexe,

a, b, c = un nombre réel positif supérieur à zéro
et $a \cdot a < 4 \cdot b$

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M = facteur d'amplification

et

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- la première et la seconde admittance de la première paire d'admittances comprennent chacune une combinaison en parallèle d'un premier condensateur ayant une valeur pratiquement égale à M/K et d'une combinaison en série d'une première résistance ayant une valeur pratiquement égale à $K/A/M$ et d'un second condensateur ayant une valeur pratiquement égale à $M \cdot A/(c \cdot K)$

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- la première et la seconde admittance de la seconde paire d'admittances comprennent chacune une combinaison en parallèle d'une seconde résistance ayant une valeur pratiquement égale à $K/M \cdot b/d$ et d'une combinaison en série d'une troisième résistance ayant une valeur pratiquement égale à $-K/B/M$ et d'un troisième condensateur ayant une valeur pratiquement égale à $-B \cdot M/(d \cdot K)$;

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- la première et la seconde admittance de la troisième paire d'admittances comprennent chacune une combinaison en parallèle d'une quatrième résistance ayant une valeur pratiquement égale à $K \cdot b/d$ et d'un condensateur ayant une valeur pratiquement égale à $1/K$;

- la première et la seconde admittance de la quatrième paire d'admittances comprennent chacune une combinaison en série d'une cinquième résistance ayant une valeur pratiquement égale à $-K/C$ et d'un cinquième condensateur ayant une valeur pratiquement égale à $-C/(d \cdot K)$,

où d est un nombre réel positif supérieur à c ,

$$A = 2 \cdot (c \cdot c + a \cdot c + b)/(d - c)$$

$$B = -(d + a + b/d)(d + c)/(d - c)$$

$$C = -(d - a + b/d)$$

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et K est un nombre réel positif.

7. Circuit de filtrage équilibré suivant l'une quelconque des revendications précédentes, caractérisé en ce qu'au moins une desdites admittances est composée d'un réseau RC équivalent ayant pratiquement la même admittance.

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