ABSTRACT

A digital demodulator which demodulates information signals that have been phase-modulated using a method such as PSK (Phase Shift Keying). The adder 46 adds a compensation value held by the phase compensator 45 to phase difference data outputted from the comparator 43. The subtractor 47 subtracts phase difference data delayed by the delaying circuit 44 by one information symbol period from the sum of the phase difference data and the compensation value from the adder 46, thus performing delay detection. With this digital demodulator, an input signal can be received and demodulated even if its frequency is not an integral division of the frequency of a master clock signal, and an oscillator can be used even if its frequency is not an integral multiple of the frequency of an input signal to be demodulated.