CLAIMS

1. A semiconductor memory, comprising:

a plurality of storage arrays;

at least one verification module, wherein each verification module of the at least one verification module corresponds to storage arrays of the plurality of storage arrays, the each verification module is configured to verify whether an error occurs in data information of the corresponding storage arrays, and the each verification module is connected to a group of global data buses; and

a plurality of gating circuits, wherein the gating circuits are connected between the storage arrays and the global data buses, and the gating circuits are configured to control on and off of a data transmission path connecting the global data buses to the storage arrays;

wherein the semiconductor memory comprises a first array, a second array and a third array; the second array is connected to two second gating circuits, and each of the two second gating circuits is connected with a corresponding one of the global data buses;

wherein the first array is connected to at least a first gating circuit, the third array is connected to at least a third gating circuit,

wherein the first gating circuit, the second gating circuit and the third gating circuit, which are connected to a same global data bus, are turned on at different time.

2. The semiconductor memory according to claim 1, wherein the second array comprises a first bit line and a second bit line, the first bit line is connected to one of the two second gating circuits, and the second bit line is connected to the other of the two second gating circuits.

3. The semiconductor memory according to claim 1, wherein the first array is connected to two first gating circuits, and the first gating circuits are connected in one-to-one correspondence to the global data buses;

the third array is connected to two third gating circuits, the third gating circuit is connected in one-to-one correspondence to the global data buses.

4. The semiconductor memory according to claim 1, wherein the verification module comprises:

a coding unit, which is connected to the storage array, and is configured to receive input data information, encode the data information to generate written verification information, and send the data information and the written verification information to the storage arrays; and

an error detection unit, which is connected to the storage arrays, and is configured to synchronously read the data information and the written verification information from the storage arrays, and verify whether an error occurs in the read data information according to the written verification information.

5. The semiconductor memory according to claim 4, wherein the error detection unit is further connected to the coding unit, the coding unit is further configured to encode the read data information to generate the read verification information, and send the read verification information to the error detection unit;

the error detection unit is configured to obtain the written verification information and the read verification information, and compare the written verification information with the read verification information to judge whether the error occurs in the read data information.

6. The semiconductor memory according to claim 5, wherein the verification module further

includes an error correction unit, the error correction unit is connected to the error detection unit, and is configured to receive the read data information and comparison result information of the error detection unit, and update the data information according to the comparison result information.

7. The semiconductor memory according to claim 1, wherein the semiconductor memory further comprises a gating control module, which is configured to generate a plurality of gating signals;

the gating circuits comprise switch transistors, control ends of the switch transistors are connected to the gating control module, first ends of the switch transistors are connected to the global data buses, second ends of the switch transistors are connected to the storage arrays, and the switch transistors are configured to select to turn on or off the data transmission path between the first ends and the second ends under the control of the gating signals.

8. The semiconductor memory according to claim 7, wherein the switch transistors are high-voltage switch transistors.

9. The semiconductor memory according to claim 7, wherein the switch transistors are turned on when the control ends of the switch transistors receive high-level signals.

10. The semiconductor memory according to claim 1, wherein the semiconductor memory further comprises at least one byte data port, the byte data port is connected in one-to-one correspondence to the verification modules, and the byte data port is configured to receive data information input from outside or output the read data information to outside.

11. The semiconductor memory according to claim 1, wherein the semiconductor memory

further comprises a read-write control module, which is connected to the verification module and the global data bus respectively; the read-write control module is configured to receive a read-write enable signal, and select a data transmission direction between the verification module and the corresponding global data bus under the control of the read-write enable signal.