

SPECIFICATION

Transistor power amplifier circuit

5 The present invention relates to a transistor power amplifier circuit including a push-pull output circuit. 5

Output transistors used in a transistor power amplifier circuit must be operated within an Area of Safety Operation region (Area of Safety Operation hereinafter abbreviated to ASO) so that permanent secondary breakdown does not occur in the collector/emitter voltage V_{CE} against collector current I_C characteristic. If the point of operation of the transistor moves out of the ASO region, the transistor develops secondary breakdown and is irreparably damaged. 10

If the temperature at the collector/base junction of the transistor increases above a maximum junction temperature, thermal runaway occurs in the collector current whereby secondary breakdown develops in the transistor. The temperature at the collector/base junction of the transistor varies in proportion to the power loss at the collector/base junction. 15

However, the power loss of the transistor is equal to the root-mean-square value of the product of the voltage V_{CE} across the collector and emitter electrodes and a collector-current I_C . Therefore, the D.C. power loss $P_d(DC)$ of a transistor which operates with a constant collector/emitter voltage V_{CE} and with a constant collector current I_C , is greater than the A.C. power loss $P_d(AC)$ of a transistor which operates with an instantaneous collector/emitter voltage V_{CE} and with an instantaneous collector current I_C . 20

Hence, referring to collector/emitter voltage V_{CE} against collector current I_C characteristics of a transistor as shown in Fig. 4 of the accompanying drawings, a D.C. ASO region ASO_{DC} in which the transistor operates with a constant voltage V_{CE} and with a constant current I_C is narrower than an A.C. ASO region ASO_{AC} in which the transistor operates with an instantaneous value V_{CE} and with an instantaneous value I_C . 25

In a push-pull output circuit which operates on a positive power-supply voltage V_{CC} and which drives a load resistor R_L via an output coupling capacitor, it is normal that two output transistors connected in series between a power-supply voltage V_{CC} and earth potential GND are D.C. biased so that a voltage of about $V_{CC}/2$ is applied across the collector and emitter electrodes of each of the transistors when no A.C. signals are introduced. 30

When an output voltage of the push-pull output circuit is raised and lowered in response to the input signals, with the D.C. operation level of $V_{CC}/2$ as a centre, and when the input signals do not cause the voltage to rise to the power-supply voltage V_{CC} and do not cause the voltage to lower to earth potential GND, the output of the push-pull amplifier circuit has a non-clipped form. Under the non-clipped output condition, the locus of operation, determined by the collector/emitter voltage V_{CE} against collector current I_C characteristic of a single output transistor, does not exceed a straight line Z_1 connecting the two operation points $[0(V), V_{CC}/2R_L(A)]$ and $[V_{CC}(V), 0(A)]$, as shown in Fig. 4. 35

However, when excessive input signals are applied, the two output transistors are alternately rendered conductive and non-conductive in response to the input signals. Therefore, the output of the push-pull output amplifier circuit is raised to the power-supply voltage V_{CC} and is lowered to earth potential GND in response to the input signals, thereby to produce pulse waveforms clipped between the two voltage levels. Under the clipped condition, the two output transistors perform a switching operation between the two levels, i.e., between the power-supply voltage V_{CC} and earth potential GND. However, the locus of operation of a single output transistor under the clipped output condition does not exceed a straight line Z_2 connecting the two operation points $[0(V), V_{CC}/R_L]$, $[V_{CC}(V), 0(A)]$ as shown in Fig. 4. 40

Therefore, in the case of A.C. operation of the output transistor of the push-pull output circuit, the operation locus may move outside the A.C. ASO region ASO_{AC} due to a variety of reasons, causes the occurrence of permanent secondary breakdown of the output transistor. If the base current of the output transistor is so controlled that the operation locus of the output transistor is confined within a restriction level Z in the A.C. ASO region ASO_{AC} , it is possible to prevent the output transistor from being irreparably damaged. For this purpose, a protecting circuit must detect any operation locus of the output transistor which has moved outside the level Z , and must also control the base current of the output transistor so that the operation locus of the output transistor is confined within the level Z . 45

In order to increase the maximum output power of the transistor power amplifier circuit including the push-pull output circuit, the detection-restriction level Z and the operation locus Z_2 under the clipped condition must be brought as close as possible to a limiting line of the A.C. ASO region ASO_{AC} . 50

When the detection-restriction level Z of the protecting circuit for protecting the output transistor and the A.C. operation locus Z_2 under the clipped condition come very close to the limit line of the A.C. ASO region ASO_{AC} , the output transistor of the transistor power amplifier circuit is very likely to develop permanent secondary breakdown. 55

Thus, when the output terminals of the push-pull output circuit are D.C. short-circuited, the operation locus Z_s of the D.C. short-circuit is as shown in Fig. 4. Due to the detection-restriction level 2 of the protecting circuit, the D.C. operation point P_s of the output transistor when the output terminals are D.C. short-circuited is restricted to a point at which the detection-restriction level 2 meets the operation locus Z_s when the output terminals are D.C. short-circuited as shown in Fig. 4.

As is clear from Fig. 4, however, the D.C. operation point P_s when the output terminals are D.C. short-circuited is likely to be located outside the D.C. ASO region ASO_{DC} . In such a case, the temperature at the collector/base junction of the output transistor will exceed a maximum junction temperature, giving rise to the occurrence of permanent secondary breakdown.

According to the present invention there is provided a transistor power amplifier circuit including:

- a first output transistor connected between a first potential and a first output terminal;
- a second output transistor connected between said first output terminal and a second potential;
- a drive circuit for driving said first and second output transistors in a push-pull manner;
- an operation detector circuit for detecting the operation of said first output transistor;
- a level detector circuit for detecting the D.C. voltage level of said first output terminal; and
- a control circuit which is controlled by the detection outputs of said operation detector circuit and said level detector circuit thereby to control said drive circuit;
- said operation detector circuit detecting the operation of said first output transistor when it has deviated beyond a predetermined detection level which is set between a locus of A.C. operation of said first output transistor when operating under a clipped condition and an A.C. safety operation region of said first output transistor, said level detector circuit detecting the D.C. voltage level of said first output terminal when it is D.C. short-circuited to said second potential, and said drive circuit restricting the operation of said first output transistor within a restriction level which is set within a D.C. safety operation region of said first output transistor in accordance with an output of said control circuit when the operation of said first output transistor deviates beyond said predetermined level or said first output terminal is D.C. short-circuited to said second potential.

The present invention will now be described in greater detail, by way of example, with reference to the remaining figures of the accompany drawings, wherein:

Figure 1 is a circuit diagram showing a first embodiment of a transistor power amplifier circuit according to the present invention;

Figure 2 is a circuit diagram showing a second embodiment of a transistor power amplifier circuit according to the present invention;

Figure 3 is a circuit diagram showing a third embodiment of a transistor power amplifier circuit according to the present invention; and

Figure 5 shows a Balanced Transformer-Less circuit (hereinafter abbreviated to BTL circuit) in which the transistor power amplifier circuit according to the third embodiment shown in Fig. 3 is constructed in the form of a monolithic semiconductor integrated circuit.

Referring first to Fig. 1, the transistor power amplifier circuit includes transistors Q_{16} and Q'_{14} which form a push-pull output circuit. When no A.C. signals are being introduced, the collector and emitter electrodes of each of the transistors Q_{16} and Q'_{14} are D.C. biased so that a voltage of about $V_{CC}/2$ which is one-half of the power-supply voltage V_{CC} is applied thereto.

A drive circuit 1 for driving push-pull output transistors Q_{16} and Q'_{14} is composed of a large-amplitude class-A amplifier circuit and a biasing circuit.

The voltage across the collector and emitter electrodes of the output transistor Q_{16} is applied to terminals t_1 and t_2 of an operation detector circuit 2 and a signal converted from the emitter current, which is approximately equal to the collector current, by means of a resistor R_8 is applied to a terminal t_3 , such that the detection level Z is set within an A.C. ASO region ASO_{AC} as shown in Fig. 4.

When there is no abnormal condition, such as D.C. short-circuiting of an output terminal T_3 , the D.C. voltage at the output terminal T_3 of the push-pull output circuit acquires a value of nearly $V_{CC}/2$.

According to the first embodiment, the operation detector circuit 2 produces an output signal of logic level "1" when the operation locus of the output transistor Q_{16} is within the detection level Z and a D.C. voltage detector circuit 3 produces an output signal of logic level "1" when the D.C. voltage of the output terminal T_3 is approximately $V_{CC}/2$.

An AND circuit 4, to which the outputs of the two detector circuits 2 and 3 are applied, forms a control circuit. The drive circuit 1 is controlled by the output of the AND circuit 4. When the output of the AND circuit 4 is at the logic level "0", both of the output transistors Q_{16} and Q'_{14} are rendered non-conductive.

On the other hand, when the push-pull output transistor Q_{16} is operating within the detection level Z , the detection output of the operation detector circuit 2 and the detection output of the

D.C. voltage detector circuit 3 acquires a logic level "1", and thus the AND circuit 4 produces an output of logic level "1". In this case, the drive circuit 1 drives the output transistors Q_{16} and Q'_{14} in response to an input signal IN applied to an input terminal T_1 .

When the output terminal T_3 is D.C. short-circuited to earth potential GND, due to short-circuit in the load for example, the operation locus of the output transistor Q_{16} moves outside the detection level Z. Hence, the detection output of the detector circuit 2 is changed from logic level "1" to logic level "0", so that the output of the AND circuit 4 correspondingly acquires logic level "0". Consequently, the drive circuit 1 causes the output transistors Q_{16} and Q'_{14} to be non-conductive. Therefore, the detection output of the operation detector circuit 2 is restored to the logic level "1". However, when the output terminal T_3 is D.C. short-circuited to earth potential GND the potential of the output terminal T_3 remains approximately at the earth potential, and the detection output of the d-c voltage detector circuit 3 acquires the logic level "0". Due to the logic level "0" of the detector circuit 3, the output of the AND circuit 4 acquires the logic level "0", such that the output transistors Q_{16} and Q'_{14} are maintained in the non-conductive state.

According to the first embodiment, therefore, the detection level Z of the operation detector circuit 2 has been set to lie in the A.C. ASO region ASO_{AC} as shown in Fig. 4. Hence, when the output terminal T_3 is D.C. short-circuited to earth potential GND, causing the operation locus of the output transistor Q_{16} to exceed the detection level Z, the output transistors Q_{16} and Q'_{14} are controlled to operate within a restriction level Z' in which the power loss is very much smaller than the power loss in the detection level Z as shown in Fig. 4. The power loss in the restriction level Z' is set to a value smaller than the power loss in the D.C. ASO region ASO_{DC} . Therefore, the output transistors Q_{16} and Q'_{14} are controlled to change to a cut off state. Consequently, the restriction level Z' corresponds to a leakage current I_{CEO} between the collector and the emitter electrodes when the base of the transistor is conducting.

When the output terminal T_3 is D.C. short-circuited to earth potential GND, the D.C. operation point Ps' is located in the D.C. ASO region ASO_{DC} of the output transistor as shown in Fig. 4. It therefore protects the output transistor Q_{16} from being irreparably damaged.

According to the first embodiment, a leakage current is supplied from the power supply V_{CC} to the output terminal T_3 , due to the ASO protecting circuit 2. Hence, when the short-circuited state is removed a D.C. blocking capacitor C or a parasitic capacitance connected to the output terminal OUT is electrically charged by the leakage current circuit; the D.C. potential at the output terminal T_3 rises to $V_{CC}/2$.

Due to the rise of the D.C. voltage, the detection output of the detector circuit 3 acquires logic level "1". Also, since the detection output of the detector circuit 2 has already been restored to logic level "1", the output of the AND circuit 4 acquires logic level "1", so that the output transistors Q_{16} and Q'_{14} are automatically changed from the non-conductive state. A complicated automatic restoration circuit is needed when it is desired to maintain the output transistors Q_{16} and Q'_{14} in the non-conductive state by applying the detection output to a latch circuit. Therefore, the first embodiment of the present invention is also advantageous in this respect.

According to the first embodiment, when the detection output of the detector circuit 2 acquires logic level "0" with respect to the short-circuited output terminal as a result of the short-circuiting across the load resistor R_L connected to the D.C. blocking capacitor C, the output of the AND circuit acquires logic level "0" and the output transistors Q_{16} , Q'_{14} are rendered non-conductive. Since the output level of the detector circuit 3 remains in logic level "1" with respect to the A.C. short-circuiting of the output terminal T_3 to earth potential GND, the turn-off of the output transistors Q_{16} and Q'_{14} causes the detection output of the detector circuit 2 to acquire logic level "1", and hence the output of the AND circuit acquires logic level "1". Therefore, the output transistors Q_{16} and Q'_{14} operate again. Thus, this operation is repeated for each short-circuiting of output which occur alternately.

According to a second embodiment of the present invention shown in Fig. 2, the repeating period can be extended, and the D.C. voltage detector circuit can be constructed in a simplified manner.

According to the second embodiment, the D.C. voltage detector circuit consists of a time-constant circuit made up of a resistor R_{12} and a capacitor C_1 connected between the output terminal T_3 and earth potential GND; the output voltage of the capacitor C being applied via the resistor R_{12} . The charging voltage of the capacitor C_1 is applied to a Schmitt trigger circuit 5, and the output transistors Q_{16} and Q'_{14} are rendered non-conductive by controlling the drive circuit 1 by means of the output of the Schmitt trigger circuit 5.

With this second embodiment, the detector circuit 2 operates when the output terminals are D.C. short-circuited and hence the Schmitt trigger circuit 5 is reversed to control the drive circuit 1, and the output transistors Q_{16} and Q'_{14} are rendered non-conductive. When the output terminals are D.C. short-circuited, the capacitor C_1 is not electrically charged by the leakage current through the detector circuit 2 and the resistor R_{12} . Under this condition, since the

Schmitt trigger circuit 5 retains the reversed state, the protecting operating is continuously maintained.

However, when the output terminals are changed from the D.C. short-circuited state, the capacitor C_1 is electrically charged by the leakage current which flows through the detector circuit 2 and the resistor R_{12} ; the Schmitt trigger circuit 5 is reversed again, and the amplification operation is automatically restored.

When the output terminal T_3 is A.C. short-circuited, the repetitive operation is defined by the hysteresis level of the Schmitt trigger circuit 5, and by the time constant determined by the resistor R_{12} and the capacitor C_1 . Hence, the period of repetition is lengthened, and less electric power is consumed by the output transistors Q_{16} and Q'_{14} . According to the second embodiment, the detection level Z of the detector circuit 2 can be brought near the limit of the A.C. ASO region ASO_{AC} , which is very useful for forming a power amplifier circuit of high power output.

Also, the transistor power amplifier circuit according to the second embodiment, consists of the ASO detector circuit of the embodiment shown in Fig. 1 to which are added the capacitor C_1 , the resistor R_{12} and the Schmitt trigger circuit 5. Therefore, the circuit setup can be simplified.

Fig. 3 is a circuit diagram showing a third embodiment according to the present invention, which is constructed in the form of a monolithic integrated circuit.

Large-amplitude class-A amplifier transistors Q_6 and Q_7 are connected in a Darlington configuration and receive inputs which have been converted into current signals through a pre-amplifier 6.

A quasi-complementary push-pull output circuit is formed by transistors Q_{15} , Q_{16} , Q_{13} and Q_{14} , which receive output voltages of large amplitudes from the transistors Q_6 and Q_7 .

A circuit for biasing the output transistors Q_{13} , Q_{15} is formed firstly by a transistor Q_8 which has its base and emitter electrodes connected together, and is connected between the base electrodes of the transistors Q_{13} and Q_{15} , secondly by a transistor Q_9 connected to the emitter electrode of the transistor Q_{13} , and thirdly by diodes Q_{10} to Q_{12} .

A constant-current load is formed by a transistor Q_4 connected to the collector electrodes of the transistors Q_6 and Q_7 in the drive stage.

The transistor Q_5 , the base electrode of which is connected to the base electrode of the transistor Q_4 , supplies a constant current to the diodes Q_{10} to Q_{12} which form part of the biasing circuit.

These transistors Q_4 and Q_5 are driven by a transistor Q_3 with its base and collector electrodes connected together. The transistor Q_3 receives constant-current outputs from transistors Q_1 and Q_2 which form a current mirror circuit which receives a current from a constant-current circuit 10.

A detector circuit for detecting the operation (voltage across the collector and emitter electrodes, and collector current or emitter current) of the output transistor Q_{16} is formed firstly by voltage-dividing resistors R_6 and R_7 connected across the collector and emitter electrodes of the output transistor Q_{16} , secondly by an emitter resistor R_8 , thirdly by a transistor Q_{17} . The collector output of the transistor Q_{17} is supplied to a current mirror circuit consisting of transistors Q_{18} and Q_{19} , and the output current of the current mirror circuit flows through a resistor R_{11} . A transistor Q_{22} is actuated by a voltage provided by the resistor R_{11} . The transistor Q_{22} establishes a circuit for electrically discharging a capacitor C_1 which forms an element of a time-constant circuit.

A resistor R_{12} for detecting the D.C. voltage is connected between the capacitor C_1 and the output terminal T_3 , thereby to form a time-constant circuit together with the capacitor C_1 .

A Schmitt trigger circuit is formed by transistors Q_{20} and Q_{21} of which the emitter electrodes have been connected together by collector resistors R_{14} and R_{15} , and by emitter resistors R_{16} and R_{17} . The Schmitt trigger circuit produces an output with a hysteresis characteristic at a connection point between the resistor R_{16} and the resistor R_{17} relying upon different emitter currents of the transistors Q_{20} , Q_{21} which operate with a hysteresis characteristic, depending upon the resistances of collector resistors R_{14} and R_{15} .

A transistor Q_{23} which receives a voltage divided by the above resistors R_{16} and R_{17} , provides a protecting function.

During the protecting operation, the protecting transistor Q_{23} is rendered conductive, and hence its collector electrode operates to short-circuit the base and emitter electrodes of the transistor Q_1 on the input side of the constant-current circuit and renders the transistor Q_1 non-conductive. When the transistor Q_1 is non-conductive, the constant-current transistors Q_4 and Q_5 are rendered non-conductive, and the output transistors Q_{16} and Q_{14} are also rendered non-conductive.

In the third embodiment, immediately after the power supply V_{CC} is turned on, the D.C. detection output will be at earth potential, similarly to the case when the D.C. load is short-circuited. Hence, when the protecting circuit is operated, the output terminal T_3 may exhibit a poor response in output potential with the rise in power supply. Such a condition may develop

when the load R_L is connected to the output terminal T_3 via a D.C. blocking capacitor C , or when a capacitive load is connected thereto. In order to prevent this condition, a transistor Q_{24} is connected in series with the protecting transistor Q_{23} , and is controlled by way of power-supply voltage detector consisting of a zener diode ZD . Thus before the power-supply voltage V_{CC} reaches the zener breakdown voltage V_Z of the zener diode ZD , the transistor Q_{24} is turned off in order to prevent the operation of the protecting circuit when the power supply is turned on.

In the third embodiment, another output transistor Q_{14} is also rendered non-conductive during the protecting operation, because it is necessary to perform the automatic restoration operation when the D.C. short-circuit condition is removed.

The present invention is not restricted to the three embodiments described. In the circuit of Fig. 1, for example, the AND circuit 4 may be replaced by an OR circuit, a NAND circuit, a NOR circuit, depending upon the logic level for detecting the operation of the output transistor or the logic level for detecting the D.C. voltage. Also, referring to the circuit of Fig. 2, the Schmitt trigger circuit may simply be a voltage comparator circuit.

Moreover, the operation detector circuit 2 may be variously modified, and the push-pull output circuit and the drive circuit therefor can also be varied in a variety of ways.

Fig. 5 shows a fourth embodiment of the present invention in which the protecting circuit of the present invention is applied to a BTL circuit made up of the push-pull output amplifier circuit in the form of a monolithic semiconductor integrated circuit according to the third embodiment shown in Fig. 3.

The circuit elements surrounded by a broken line are all formed in a single silicon chip by the conventional method of making semiconductor integrated circuits.

An input signal applied to an input terminal T_9 is transmitted to an input terminal T_1''' of the integrated circuit. A differential phase separator circuit 100 consisting of transistors Q_{31} to Q_{33} and resistors R_{31} to R_{34} , operates in response to the input signals and produces two output signals with an anti-phase relation, onto two signal lines Z_{10} and Z_{11} . The value of constant current flowing through the constant-current transistor Q_{33} of the differential phase separator circuit 100 is determined by a biasing current which flows in a biasing circuit 101 made up of a transistor Q_{34} and a resistor R_{35} .

A zener diode ZD' , a resistor R_{36} and a transistor Q_{35} form a constant-voltage regulator 102 which generates an operation voltage of approximately a constant value irrespective of the power-supply voltage V_{CC} fed to the power-supply terminal T_2 .

The operation voltage is fed to the differential phase separator circuit 100 and to the biasing circuit 101 via a resistor R_{37} .

The BTL circuit also includes a pair of power amplifier circuits 103 and 103' for directly driving a speaker SP without interposing any output coupling capacitors. The pair of power amplifier circuits 103 and 103' are constructed to have the same form and therefore, only one power amplifier circuit 103 is shown in detail.

The speaker SP is directly connected between a pair of output terminals T_{213} and T'_3 of the pair of power amplifier circuits 103 and 103'.

To prevent oscillation, a series circuit, consisting of a capacitor C_{101} and a resistor R_{101} , is connected in parallel with the speaker SP , a series circuit consisting of a capacitor C_{102} and a resistor R_{102} is connected between the output terminal T_3 and an earth terminal T_4 , and a series circuit consisting of a capacitor C'_{102} and a resistor R'_{102} is connected between the output terminal T'_3 and the earth terminal T_4 .

Bootstrap capacitors C_{103} and C'_{103} are connected between output terminals T_3 and T'_3 and bootstrap terminals T_5 and T'_5 respectively.

The two signals sent onto the two signal lines Z_{10} and Z_{11} are applied to the base electrodes of transistors Q_{36} and Q'_{36} in initial-stage amplifier circuits 104 and 104', of the pair of power amplifier circuits 103 and 103'.

The initial-stage amplifier circuit 104 includes a modified differential amplifier circuit consisting of transistors Q_{36} and Q_{37} and a resistor R_{38} , a current mirror circuit consisting of transistors Q_{38} and Q_{39} , and a load consisting of the resistor R_{40} as shown. An approximately constant operation voltage is applied by a constant-voltage regulator 102 to the initial-stage amplifier circuit 104 via a resistor R_{39} . One end of the resistor R_{39} is connected via a terminal T_6 to a filter capacitor C_{104} for removing power-supply rippling whereby the differential phase separator circuit 101 is allowed to operate in a stable mode.

An output OUT produced from the output terminal T_3 of the power amplifier circuit 103 is transmitted to the base electrode of the transistor Q_{37} of the initial-stage amplifier circuit 104 via a negative feedback circuit 105 consisting of resistors R_{41} and R_{42} , a constant-current transistor Q_{40} , and a capacitor C_{105} which is connected between earth and the junction between the resistor R_{42} and the collector electrode of the transistor Q_{40} via a terminal T_7 , whereby an A.C. voltage gain of the power amplifier circuit 103 is determined, and a D.C. output voltage level at the output terminal T_3 of the power amplifier circuit 103 is determined so as to acquire a value

of nearly $V_{CC}/2$.

The base electrode of the constant-current transistor Q_{40} is biased by a biasing circuit 106 consisting of a transistor Q_{41} and a resistor R_{44} . Since the biasing circuit 106 is connected to the power-supply terminal T_2 , a constant current which flows into the constant-current transistor Q_{40} is dependent upon the power-supply voltage V_{CC} . Therefore, even when the power-supply voltage V_{CC} is varied, the D.C. output level at the output terminal T_3 follows the value $V_{CC}/2$ which varies in response to the changes in the power-supply voltage V_{CC} .

Also, the output signal of the initial-stage amplifier circuit 104 produced across the resistor R_{40} is amplified by a drive amplifier circuit consisting of transistors Q_6 and Q_7 connected in Darlington configuration, a resistor R_1 , a phase compensating capacitor C_{106} , a transistor Q_8 with its base and collector electrodes connected together, a resistor R_3 , and a constant-current load transistor Q_4 . The output of the drive amplifier circuit 107 is fed to the transistors Q_{15} and Q_{16} connected in Darlington configuration, in the push-pull output amplifier circuit 108, and also to complementary-connected transistors Q_{13} and Q_{14} .

The emitter electrode of the transistor Q_{13} is connected to an idling current adjusting circuit 109 consisting of diodes Q_{10} to Q_{12} , and transistors Q_9 and Q_5 , such that the crossover distortion of the push-pull output amplifier circuit 108 can be reduced.

The base electrode of the constant-current load transistor Q_4 of the drive amplifier circuit 107 and the base electrode of the transistor Q_5 of the idling current adjusting circuit 109 are connected to the base electrode of the transistor Q_3 of the biasing circuit 110. The biasing circuit 110 consists of transistors Q_1 and Q_2 , and a resistor R_{45} , and is operated by an approximately constant operation voltage from a constant-voltage regulator 102. Therefore, the D.C. biasing current flowing into the drive amplifier circuit 107 and a D.C. biasing current flowing into a push-pull output amplifier circuit 108 are maintained at approximately constant values despite the changes in power-supply voltage V_{CC} .

A detector circuit 2 for detecting the operation of the output transistor Q_{16} is constructed by means of transistors Q_{42} to Q_{44} and resistors R_6 to R_8 and R_{48} .

One end of the resistor R_{48} and the base electrode of the transistor Q_{44} are connected to the collector electrode of the transistor Q_{45} . The other end of the resistor R_{48} and the collector electrode of the transistor Q_{44} are connected to the base electrode of the control transistor Q_{46} . The emitter electrode of the control transistor Q_{46} is connected to one end of the resistor R_8 . The collector electrode of the control transistor Q_{46} is connected to the collector electrode of the transistor Q_{47} . The base electrodes of the transistors Q_{45} and Q_{47} are connected to the base electrode of the transistor Q_{48} in the biasing circuit 112.

The biasing circuit 112 also includes a transistor Q_{49} and a resistor R_{49} . The power-supply voltage V_{CC} is supplied to one end of the resistor R_{49} via a power-supply terminal T_2 .

The collector electrode of the control transistor Q_{46} is connected to the base electrode of transistor Q_{22} .

The collector electrode of the transistor Q_{22} in the power amplifier circuit 103 and the collector electrode of the transistor Q'_{22} in the power amplifier circuit 103' are connected to a capacitor C_1 via the terminal T_8 . Since the transistors Q_{22} and Q'_{22} are usually rendered non-conductive, the capacitor C_1 is electrically charged to a D.C. operation voltage $V_{CC}/2$ supplied from the output terminals T_3 , T'_3 due to resistors R_{12} , R'_{12} and R_{50} .

The terminal T_8 is also connected to an input of a Schmitt trigger circuit 5 via a resistor R_{13} . The Schmitt trigger circuit 5 comprises transistors Q_{20} and Q_{21} and resistors R_{14} to R_{17} . The output of the Schmitt trigger circuit is obtained at the junction between the resistor R_{16} and the resistor R_{17} . The resistance of the resistor R_{14} has been set to be, for example, 10 kilohms which is greater than the resistance (for example, 2 kilohms) of the resistor R_{15} , such that the output of the trigger circuit acquires a low level when the capacitor C_1 has been electrically charged.

The detector circuit 2, however, is so designed that the detection level Z lies between the operation locus Z_2 of the output transistor Q_{16} and the A.C. ASO region ASO_{AC} , similar to the characteristics shown in Fig. 4.

Thus, the constant current I_0 which flows into the transistor Q_{45} is given by the relation;

$$I_0 = V_{CC} - (V_{BEQ48} + V_{BEQ49})/R_{49} \quad (1)$$

where V_{CC} represents the power-supply voltage V_{CC} , V_{BEQ48} and V_{BEQ49} represent forward voltages across the base and emitter electrodes of the transistors Q_{48} and Q_{49} , and R_{49} the resistance of the resistor R_{49} .

When the resistors R_6 to R_8 satisfy the requirement $R_6 \gg R_7 \gg R_8$, the voltage V_{BEQ46} appearing across the base and emitter electrodes of the control transistor Q_{46} is given by the following relation, which is similar to the equation (3) described previously.

$$V_{BEQ46} \approx I_{CQ16} R_8 + R_7/R_6 (V_{CEQ16} - V_{BEQ42} - V_{BEQ43}) + I_0(R_7 - R_{48}) + V_{BEQ44} \quad (2)$$

where B_{BEQ46} and V_{BEQ47} represent forward voltages across the base and emitter.
From relations (1) and (2),

$$5 \quad V_{BEQ46} \approx I_{CQ16} R_8 + R_7/R_6 (V_{CEQ16} - V_{BEQ42} - V_{BEQ43}) + (R_7 - R_{48})/R_{49} [V_{CC} - (V_{BEQ48} + V_{BEQ49})] + V_{BEQ44} \dots (3) \quad 5$$

The resistances are set so that the resistors R_6 to R_8 satisfy the requirement $R_6 \gg R_7 \gg R_8$, the resistors R_7 and R_{48} satisfy the requirement $R_{48} = 2R_7$, and the resistors, R_6 , R_7 , R_{48} and R_{49} satisfy the requirement $R_7/R_6 = (R_7 - R_{48})/R_{49}$.

- 10 $R_6 = 10$ kilohms (semiconductor resistor),
 $R_7 = 100$ ohms (semiconductor resistor).
 $R_8 = 15$ milliohms (equivalent resistance in the layer of aluminium wiring),
 $R_{48} = 200$ ohms (semiconductor resistor),
 15 $R_{49} = 10$ kilohms (semiconductor resistor). 15

Hence, if the base/emitter junction characteristics of the transistors Q_{42} and Q_{43} are equal to the base/emitter junction characteristics of the transistors Q_{48} and Q_{49} , the current-limiting equation (conditions in which a relation $V_{BEQ46} > V_{BEQ44}$ is satisfied, and the control transistor Q_{46} is rendered conductive) obtained from the equation (3) can be written as follows:— 20

$$I_{CQ16} R_7/R_6 R_8 (V_{CC} - V_{CEQ16}) \dots (4)$$

As is clear from the current-limiting equation (4), the dispersion in base-emitter junction characteristics of the transistors Q_{48} and Q_{49} in the biasing circuit 112, and the temperature dependency, are cancelled by those of the transistors Q_{42} and Q_{43} in the detector circuit 2, and hence it is possible to obtain a line of detection level which does not depend on the base/emitter junction characteristics of the transistors. 25

Similarly to the case of Fig. 4, just before the output of the output transistor Q_{16} of the power amplifier circuit 103 exceeds the detection level Z connecting the two operating points P_1 and P_2 , the transistor Q_{22} is rendered conductive according to the equation (4), and hence the electric charge stored in the capacitor C_1 at the terminal T_8 is discharged through the transistor Q_{22} . Hence, the output of the Schmitt trigger circuit 5 at the junction between the resistor R_{16} and the resistor R_{17} acquires a high level to render the transistors Q_{23} and Q_{24} conductive, provided the power-supply voltage V_{CC} is of a sufficient value. 30

The transistors Q_{23} and Q_{24} upon being rendered conductive, cause the transistors Q_1 , Q_2 and Q_3 in the biasing circuit 110 to be non-conductive. Therefore, since the transistor Q_4 forming the constant-current load of the drive amplifier circuit 107 is rendered non-conductive, the transistors Q_{15} and Q_{16} of the push-pull output amplifier circuit 108 are rendered non-conductive. 35

Since the transistor Q_3 of the biasing circuit 110 has also been rendered non-conductive, the transistor Q_5 of the idling current adjusting circuit 109 is rendered non-conductive, and the transistors Q_{13} and Q_{14} of the push-pull output amplifier circuit 108 are rendered non-conductive. 40

Thus, the base currents of the output transistors Q_{16} and Q_{14} of the push-pull output amplifier circuit 108 are interrupted, and the operations of the output transistors Q_{16} and Q_{14} are confined within the restriction level Z' preventing them from being damaged. 45

In this case, the transistor which is rendered non-conductive in the biasing circuit 110, causes the output transistors Q'_{16} and Q'_{14} in the push-pull output amplifier circuit 108' to be non-conductive. 50

However, a serious disadvantage occurs when one terminal T_3 of the two output terminals T_3 , T'_3 of the pair of power amplifier circuits 103, 103' forming the BTL circuit is D.C. short-circuited to earth potential GND, and when the output transistors Q_{16} and Q_{14} of one power amplifier circuit 103 are rendered non-conductive, the output transistors Q'_{16} and Q'_{14} of the other power amplifier circuit 103' remain conductive. 55

Therefore, when the output transistors Q'_{16} and Q'_{14} of the other power amplifier circuit 103' remain conductive, a D.C. voltage of about $V_{CC}/2$ appears on the output terminal T'_3 while the output terminal T_3 of the power amplifier circuit 103 is D.C. short-circuited to earth potential GND. Hence, a D.C. current flows into a voice coil of the speaker SP connected across the terminals T_3 and T'_3 , so that the speaker SP may be damaged. 60

According to the fourth embodiment of the present invention, however the output transistors Q_{16} and Q_{14} , Q'_{16} and Q'_{14} of the two power amplifier circuits 103 and 103' are all rendered non-conductive under the above conditions described previously, preventing the speaker SP from being damaged.



CLAIMS

1. A transistor power amplifier circuit including:
a first output transistor connected between a first potential and a first output terminal;
a second output transistor connected between said first output terminal and a second
5 potential;
a drive circuit for driving said first and second output transistors in a push-pull manner;
an operation detector circuit for detecting the operation of said first output transistor;
a level detector circuit for detecting the D.C. voltage level of said first output terminal; and
a control circuit which is controlled by the detection outputs of said operation detector circuit
10 and said level detector circuit thereby to control said drive circuit;
said operation detector circuit detecting the operation of said first output transistor when it
has deviated beyond a predetermined detection level which is set between a locus of A.C.
operation of said first output transistor when operating under a clipped condition and an A.C.
safety operation region of said first output transistor, said level detector circuit detecting the
15 D.C. voltage level of said first output terminal when it is D.C. short-circuited to said second
potential, and said drive circuit restricting the operation of said first output transistor within a
restriction level which is set within a D.C. safety operation region of said first output transistor in
accordance with an output of said control circuit when the operation of said first output
transistor deviates beyond said predetermined level or said first output terminal is D.C. short-
20 circuited to said second potential.
2. A transistor power amplifier circuit according to Claim 1, wherein said restriction level is
set to a cut-off level of said first output transistor.
3. A transistor power amplifier circuit according to Claim 1, wherein said transistor power
amplifier circuit further includes a third output transistor connected between said first potential
25 and said second output terminal, a fourth transistor connected between said second output
terminal and said second potential thereby to execute a push-pull operation together with said
third transistor, and a speaker of which the terminals are directly connected to said first and
second output terminals, and wherein the restriction levels of said first, second, third and fourth
transistors are simultaneously controlled to the cut-off state by said control circuit during a
30 period in which said first output terminal is D.C. short-circuited to said second potential.
4. A transistor power amplifier circuit according to Claim 2 or Claim 3, wherein said
transistor power amplifier circuit further includes a constant-voltage means connected between
said first potential and said second potential, and said constant-voltage means controls said
control means so that said first output transistor is cut off when the difference between said first
35 potential and said second potential exceeds a predetermined value.
5. A transistor power amplifier circuit substantially as herein described with reference to and
as illustrated in Fig. 1 or Fig. 2 or Fig. 3 of the accompanying drawings.