AMENDED SPECIFICATION

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PATENT SPECIFICATION

947,520



DRAWINGS ATTACHED

947,520

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COMPLETE SPECIFICATION

Improvements in the manufacture of Semiconductor Devices and in Transistors made thereby

We, FAIRCHILD CAMERA AND INSTRUMENT CORPORATION, of 300 Robbins Lane, Syosset, Long Island, New York, United States of America, a corporation organized under the laws of the State of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to an improvement in the manufacture of semiconductor devices including transistors and to an improved transistor structure. More particularly, the invention relates, as to the method thereof, to the control of semiconductor diffusing and masking to the end of producing an improved diffusion transistor having fully protected junctions and maximized exposed surfaces for ohmic contact attachment.

Advancements in transistor technology have in part been directed to the production of very small sized transistor structures, inasmuch as minute semiconductor geometries are required for high frequency applications of transistors. While the well known point-contact transistor is adapted for high frequency work, yet certain limitations attach to this type of transistor and consequently junction transistors have been developed for use in the high frequency range. One type of junction transistor which is particularly well adapted for high frequency applications is the double-diffused silicon transistor, and although the present invention is adapted for use with other types of transistors it is with respect to double-diffused silicon transistors that the following description is referenced.

As regards the manufacture of double-diffused silicon transistors, and in fact any minute transistor structure, difficulty is encountered in providing a sufficient exposed area of the base material for attachment of an ohmic contact thereto. By maintaining the extremely small element dimensions required of the transistor, there results only a minute thickness of base material exposed between the base-collector junction and the emitter-base junction on a transistor surface. Conventional transistor utility requires the provision of electrical contacts to the individual transistor elements or portions, and thus it is necessary for the dimensions of the base portion to be made sufficient to attach such contacts. In certain instances this limitation upon the size of the base portion is highly undesirable, inasmuch as conventional manufacturing practices produce a base thickness in proportion to the exposed base width.

Another difficulty arising from the limited size necessary for transistors to suitably operate at very high frequencies is encountered in the difficulty of protecting the transistor junction. This is particularly noted in the attachment of electrical contacts to the transistor portions inasmuch as very minute variations in the placement of electrical conductors or ohmic contacts to the transistor may well result in electrically shorting of the transistor junction, whereby the transistor structure is unsuited for use and must be rejected. This latter problem is compounded by the necessity in high-fre-

quency transistors of employing an ohmic contact which substantially entirely covers the exposed surface of each of the elements in order to minimize the spreading resistance thereof. Conventional plating methods are unsuited for the provision of such ohmic contacts to within fractions of a millimeter from the transistor junction, as is normally required for transistor structures capable of operating at very high frequencies. Not only is the problem of providing suitable ohmic contacts to the transistor portions a major one, but also the possible damage or other types of inadvertent electrical shorting of the transistor junctions during manufacturing processes is of major importance in limiting the number of rejects in any manufacturing process. Additionally, long range contamination of transistor junctions may be a cause of drifting and deteriorization of transistor characteristics.

There have been developed for high frequency applications transistors of the "mesa" design wherein undesirable lateral extensions of the base-collector junction are removed by etching to produce transistors of very small dimensions. Although mesa transistors have found wide acceptance in the art, the junction exposed by the etching, as well as the other junction, is particularly vulnerable to contamination or degradation during subsequent portions of the manufacturing process.

According to the present invention there is provided a method of manufacturing semiconductor devices comprising the steps of forming a protective adherent mask of an electrically non-conducting compound on one substantially flat surface of a wafer of semiconductive material of a first conductivity type with a first opening in the mask exposing an area of the wafer on one plane surface thereof, diffusing an impurity wholly into the wafer surface exposed by said first opening in the mask to form a first zone of a second conductivity type of semiconductive material exposed only at said surface, the area of said first zone presented to said surface being greater than the area of said first opening in the mask whereby the junction between said semiconductive material of first conductivity type and said first zone lies beneath the mask at said surface, forming an extensional protective adherent mask of an electrically non-conducting compound during or following the diffusion step over the wafer surface exposed by said extensional mask to the mask, diffusing an impurity into the wafer surface exposed by said extensional mask to form a second zone of said first conductivity type of semiconductor material exposed only at said surface, the area of said second zone presented to said surface being greater than the area exposed by said extensional mask whereby the junction between said first and second zones lies beneath the mask at said surface, forming an opening in said extensional mask, attaching an ohmic contact to the thereby exposed portion of said first zone, attaching an ohmic contact to said second zone while permanently retaining the mask including said extensional portion thereof on the wafer surface at least covering the two junctions and attaching an ohmic contact to said semiconductive material of first conductivity type.

It is an object of the present invention to provide an improved method of manufacturing transistors wherein maximum surface protection of a device is afforded.

It is still another object of the present invention to provide an improved transistor having a protective coating thereover except for ohmic contact areas.

In the process hereof, the transistor junctions are at all times fully protected by an oxide layer or coating formed simultaneously with the junction during diffusion at high temperatures so that no contamination of the transistor junctions during or after manufacture is possible. In this manner one of the major causes of transistor failure is entirely precluded.

The present invention provides a method of transistor manufacture overcoming the above-noted problems as well as others prevalent in the art. In the manufacture of transistors it is not uncommon for the semiconducting material to become oxidized on the exterior surfaces thereof, and it is conventional during manufacture to remove this outside coating as by etching, although it has been proposed to leave a certain portion of this coating upon the transistor surface as a protection for portions thereof. The present invention provides, as integral steps in the manufacture of transistors, the control of the extent and position of semiconductor coating which serves the purpose of thereby delineating the exact lateral configuration of materials diffused into the semiconducting material and furthermore to provide a subsequent protection for the transistor surface. In accordance with the present invention it is possible not only to limit the extent of impurities diffusion in a semiconductor during the formation of different types of semiconductor, but furthermore, by the addition and subtraction of a masking layer or coating upon exposed transistor surfaces, it is herein possible to provide a precisely controlled area of any particular transistor material upon a common transistor surface. In addition, and in accordance with the present invention, there is herein provided, by the retention of a protective coating upon exposed transistor surfaces, means for preventing electrical shorting of transistor junctions and/or damage thereto during fabrication and manufacture of the transistor devices.

Various other possible objects and advantages of the present invention will become apparent to those skilled in the art from the following description of the present invention. Although the invention is herein illustrated with

respect to a particular preferred embodiment thereof, no limitation is intended thereby, and reference is made to the appended claims for a precise delineation of the true scope of the present invention.

Furthermore, although as previously noted, the present invention may be employed with a variety of semiconducting materials, yet actual use thereof has been primarily directed to silicon transistors and thus the following description is referenced thereto.

The invention is illustrated in the accompanying drawings wherein:

Figs. 1, 2, 3, 4 and 5 are sectional views through a triode semiconducting device or transistor showing same at separate stages of manufacture in accordance with the present invention; and

Fig. 6 is a sectional view through a transistor manufactured in accordance with the present invention.

Considering now the improved method of the present invention as same relates to the manufacture of double-diffused silicon transistors, reference is made to Figs. 1 to 5 of the drawing. As a first step in the manufacture there is produced a layer 31 formed, for example, of an oxide of silicon, and covering at least the upper surface of a silicon wafer 32, which may be formed of N-type silicon, for example. Preferably this coating is formed of a silicon oxide and various methods of producing such a layer are known in the art as, for example, by exposure of the silicon wafer to moisture and air, or by the utilization of an oxidizing agent such as hydrogen peroxide or the like. There is provided in this oxide layer 31 a hole or opening 33 which may be formed by photoresist techniques or by etching of the layer, as, for example, with hydrofluoric acid and the configuration of the opening in the layer 31 is controlled to define the desired configuration of the transistor base member. The apertured layer 31 serves as a mask for protecting the transistor surface and junctions and for limiting the lateral diffusion of impurities in the wafer. The layer is thus formed of a material into which impurities to be employed during transistor manufacture will not diffuse during the steps thereof, and which not only tightly adheres to the wafer surface in protective relation thereto but which also is not electrically conducting. Upon the upper surface of the wafer 32 exposed at the aperture 33 in the mask or layer 31, there is disposed a predetermined amount of acceptor impurity, as in the form of a silicon alloy, and heat is applied, as indicated by the arrows 34, whereby the impurity diffuses into the wafer 32 to form a P-type base layer 36 therein. In conventional manner there is produced through controlled heating and cooling of the transistor structure a transistor junction 37 between the base layer 36 and the wafer 32 with the upper terminus of this junction lying beneath the oxide mask 31, as illustrated in Fig. 2. As silicon technology is available in the literature, it is here only noted that N-type silicon may be formed by inclusion of an impurity chosen from Group V of the Periodic Table, while P-type silicon may be formed by inclusion of an impurity from Group II.

During or following disposition of the base layer 36 upon the wafer 32 and the formation of a transistor junction 37 therebetween, there is formed an additional or extensional portion of the oxide layer 31 in the manner previously described which is shown at 38 of Fig. 3. This additional masking 38 extends the oxide coating over an additional part of the base layer 36 to the end of masking same so that the second layer of material to be diffused into the transistor will not extend to both extremities of the base layer. With the augmented masking layer 31 upon the upper surface of the wafer 32 and in masking relation to some substantial portion of the base layer 36, there is diffused into the transistor structure a second layer 39 by the provision of a suitably impurity or alloy thereof atop the base layer and the addition of heat to raise the wafer and impurity upon same to diffusion temperature. In a conventional manner the diffusion of impurities into the wafer is precisely controlled as to rapidity and extent, so that there is thereby formed a second transistor junction 41 between an emitter layer 39 and the base layer 36. As may be seen from Fig. 4 of the drawings, the emitter 30 diffuses into the base and the junction 41 therebetween terminates at the upper surface of the wafer beneath the mask 38 adjacent the opening of reduced size therein. It will be further appreciated from the structure illustrated in Fig. 4 that there then results an uneven disposition of the second diffused layer 39 in that same is offset from the center of the base layer 36. Particular advantage is derived from this relationship of the respective layers for, as illustrated in Fig. 5, there is then removed a portion of the masking layer 31 to form an opening 42 therethrough immediately above the portion of the base layer 36 extending laterally from the emitter 39. In this manner, there is provided a substantial contact area of the base layer 36 available at the upper surface of the transistor for attachment of an ohmic contact thereto. Please note in this respect that the mask 31 is not removed from the upper surface of the transistor above the emitter-base junction 41, but instead is retained thereat so as to protect this junction from inadvertent shorting or other damage during subsequent manufacturing and handling operations. Not only is this junction 41 covered at the above-noted points, but additionally, it is wholly encased by the oxide layer 31 at all other points upon the upper surface of the wafer. Likewise, the base-collector junction 37 is fully covered by the oxide layer 31 atop the transistor. As a consequence of this struc-

ture, there is provided a materially improved transistor structure wherein inadvertent damage or shorting of the junctions thereof is wholly precluded. In a conventional manner there may then be applied ohmic contacts to the emitter, base and collector. In this respect it is herein possible to provide an ohmic contact to the collector at the upper surface thereof so as to produce a transistor having all contacts on the same side. This is herein accomplished by providing an additional opening 43 through the mask 31 in lateral separation from the base opening 42 and therefore unmasking a desired extent of the collector at the top thereof. Ohmic contacts 44, 46 and 47 are then applied in a relatively conventional manner to the separate portions of the transistor through the openings 33, 42 and 43. It is herein possible to employ conventional plating techniques to apply electrical conductors to the semiconductor. Inasmuch as the transistor junctions are entirely covered and protected upon the upper surface of the transistor, no possible electrical shorting or damage to junctions can result from plating or alloying processes.

It will of course be appreciated that the silicon oxide herein stated as comprising the masking layer 31 upon the transistor wafer 32 does not react with the impurity employed in the formation of different type semiconducting materials. In this respect particular care must be taken to exclude gallium as a suitable impurity from the Group III elements that may be diffused into the silicon, for this particular element does react with silicon oxide and consequently the mask will not be effective to limit the lateral extent of the diffusion of the impurity.

It is further noted that in the process above described relating to the manufacture of a triode transistor of a double-diffused silicon type, any unavoidable production of an oxide layer upon the upper surface of the wafer at points wherein the same is not desired is followed by the removal of same. Thus, for example, following the production of the base layer 36 by diffusing the selected impurity into the wafer 32, there may result a thin oxide layer over the top of the base portion of the transistor and this layer is then removed at least in part, as by etching or photoresist techniques.

Considering now the improved double-diffused silicon transistor of the present invention, reference is made to Fig. 6 of the drawing where there is illustrated in cross-section such a transistor. As may be seen from this figure, the improved transistor includes a collector disc or wafer 32, formed for example, of an N-type silicon. At the top of this collector wafer 32 there is disposed a thin base layer 36, formed of silicon of opposite conductive type, thus in the present example of P-type silicon. Atop the base layer 36, there is provided an emitter layer or dot 39, N-type silicon, and having a very minute dimension. Although not previously discussed, the present invention is particularly adapted to high frequency applications wherein very small dimensions are required of the transistor portions. Thus, in the present invention, the lateral extent of the emitter may be substantially less than one millimeter and the thickness of the base layer between emitter and collector may be of the order of one micron. Upon the upper surface of the wafer 32 there is provided the oxide layer or coating 31 which will be seen to fully cover both the emitter-base junction 41 and the base-collector junction 37. Openings 33, 42 and 43 through this oxide coating 31 provide communication with the emitter, base and collector, respectively, of the transistor whereby ohmic contacts may be made all in the upper plane of the transistor. Thus an ohmic contact including an electrical lead 44 is provided atop the emitter 39, while a second ohmic contact including a lead 46 is provided in connection with the upper surface of the base 36 through the masked openings 42. Likewise, a third ohmic contact 47 including an electrical conductor, is electrically and mechanically joined to the upper surface of the collector wafer 32 through the mask opening 43. The resulting transistor structure illustrated in Fig. 6 of the drawing will be seen to be particularly well adapted for high frequency applications, and furthermore to be fully protected from shorting of the junction thereof as may otherwise occur during manufacture. While this transistor structure is well adapted to the provision of an ohmic contact to the collector thereof at the common upper surface of the transistor, yet the collector contact may also be provided upon the under surface of the wafer 32.

Although the above description of both the manufacturing process and the transistor structure has been referenced to an NPN transistor, it will be appreciated that it is equally applicable to PNP type transistors.

WHAT WE CLAIM IS:—

1. A method of manufacturing semiconductor devices comprising the steps of forming a protective adherent mask of an electrically non-conducting compound on one substantially flat surface of a wafer of semiconductive material of a first conductivity type with a first opening in the mask exposing an area of the wafer on one plane surface thereof, diffusing an impurity wholly into the wafer surface exposed by said first opening in the mask to form a first zone of a second conductivity zone presented to said surface being greater than the area of said first opening in the mask whereby the junction between said semiconductive material of first conductivity type and said first zone lies beneath the mask at said surface, forming an extensional protective adherent mask of an electrically non-conducting compound during or following the diffusion step

ture, there is provided a materially improved transistor structure wherein inadvertent damage or shorting of the junctions thereof is wholly precluded. In a conventional manner there may then be applied ohmic contacts to the emitter, base and collector. In this respect it is herein possible to provide an ohmic contact to the collector at the upper surface thereof so as to produce a transistor having all contacts on the same side. This is herein accomplished by providing an additional opening 43 through the mask 31 in lateral separation from the base opening 42 and therefore unmasking a desired extent of the collector at the top thereof. Ohmic contacts 44, 46 and 47 are then applied in a relatively conventional manner to the separate portions of the transistor through the openings 33, 42 and 43. It is herein possible to employ conventional plating techniques to apply electrical conductors to the semiconductor. Inasmuch as the transistor junctions are entirely covered and protected upon the upper surface of the transistor, no possible electrical shorting or damage to junctions can result from plating or alloying processes.

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It is further noted that in the process above described relating to the manufacture of a triode transistor of a double-diffused silicon type, any unavoidable production of an oxide layer upon the upper surface of the wafer at points wherein the same is not desired is followed by the removal of same. Thus, for example, following the production of the base layer 36 by diffusing the selected impurity into the wafer 32, there may result a thin oxide layer over the top of the base portion of the transistor and this layer is then removed at least in part, as by etching or photoresist techniques.

Considering now the improved double-diffused silicon transistor of the present invention, reference is made to Fig. 6 of the drawing where there is illustrated in cross-section such a transistor. As may be seen from this figure, the improved transistor includes a collector disc or wafer 32, formed for example, of an N-type silicon. At the top of this collector wafer 32 there is disposed a thin base layer 36, formed of silicon of opposite conductive type, thus in the present example of P-type silicon. Atop the base layer 36, there is provided an emitter layer or dot 39, N-type silicon, and having a very minute dimension. Although not previously discussed, the present invention is particularly adapted to high frequency applications wherein very small dimensions are required of the transistor portions. Thus, in the present invention, the lateral extent of the emitter may be substantially less than one millimeter and the thickness of the base layer between emitter and collector may be of the order of one micron. Upon the upper surface of the wafer 32 there is provided the oxide layer or coating 31 which will be seen to fully cover both the emitter-base junction 41 and the base-collector junction 37. Openings 33, 42 and 43 through this oxide coating 31 provide communication with the emitter, base and collector, respectively, of the transistor whereby ohmic contacts may be made all in the upper plane of the transistor. Thus an ohmic contact including an electrical lead 44 is provided atop the emitter 39, while a second ohmic contact including a lead 46 is provided in connection with the upper surface of the base 36 through the masked openings 42. Likewise, a third ohmic contact 47 including an electrical conductor, is electrically and mechanically joined to the upper surface of the collector wafer 32 through the mask opening 43. The resulting transistor structure illustrated in Fig. 6 of the drawing will be seen to be particularly well adapted for high frequency applications, and furthermore to be fully protected from shorting of the junction thereeof as may otherwise occur during manufacture. While this transistor structure is well adapted to the provision of an ohmic contact to the collector thereof at the common upper surface of the transistor, yet the collector contact may also be provided upon the under surface of the wafer 32.

Although the above description of both the manufacturing process and the transistor structure has been referenced to an NPN transistor, it will be appreciated that it is equally applicable to PNP type transistors.

WHAT WE CLAIM IS:—

1. A method of manufacturing semiconductor devices comprising the steps of forming a protective adherent mask of an electrically non-conducting compound on one substantially flat surface of a wafer of semiconductive material of a first conductivity type with a first opening in the mask exposing an area of the wafer on one plane surface thereof, diffusing an impurity wholly into the wafer surface exposed by said first opening in the mask to form a first zone of a second conductivity zone presented to said surface being greater than the area of said first opening in the mask whereby the junction between said semiconductive material of first conductivity type and said first zone lies beneath the mask at said surface, forming an extensional protective adherent mask of an electrically non-conducting compound during or following the diffusion step

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over the wafer surface exposed through said first opening in the mask, diffusing an impurity into the wafer surface exposed by said extensional mask to form a second zone of said first conductivity type of semiconductor material exposed only at said surface, the area of said second zone presented to said surface being greater than the area exposed by said extensional mask whereby the junction between said first and second zones lies beneath the mask at said surface, forming an opening in said extensional mask, attaching an ohmic contact to the thereby exposed portion of said first zone, attaching an ohmic contact to the thereby exposed portion of said first zone, attaching an ohmic contact to said second zone while permanently retaining the mask including said extensional portion thereof on the wafer surface at least covering the two junctions, and attaching an ohmic contact to said semiconductive material of first conductivity type.

2. A method of manufacturing semiconductor devices as claimed in claim 1, wherein an additional opening is formed in the protective adherent mask on said surface of the semiconductor wafer over the undiffused area of semiconductive material of said first conductivity type to enable said ohmic contact to be attached to said undiffused area through said opening.

3. A semiconductor device comprising (a) a wafer mostly of a first type of conductive material (b) a first zone of a second type of conductive material beneath and exposed only on one surface of the wafer, (c) a second zone of said first type of conductive material formed within said first zone, (d) an ohmic contact attached to an area of said first type of conductive material, (e) an ohmic contact attached to an area of said first zone, (f) an ohmic contact attached to an area of said second zone and (g) a protective adherent electrically non-conducting coating formed on the wafer and masking the junction between the first type of conductive material and said first zone at said surface and masking the junction between said first zone and said second zone at said surface.

4. A method of manufacturing semiconductor devices substantially as herein before described.

5. A semiconductor device substantially as hereinbefore described and as illustrated in Figs. 1, 2, 3, 4, 5 and 6 of the accompanying drawings.

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