

RESISTIVE RANDOM ACCESS MEMORY AND MEMORY MINI-ARRAY THEREOF WITH IMPROVED RELIABILITY

Abstract of Disclosure

A memory includes a first switch transistor, a second switch transistor, a third switch transistor, a fourth switch transistor, a first resistive memory element and a second resistive memory element. Each of the first switch transistor, the second switch transistor, the third switch transistor and the fourth switch transistor includes a drain terminal, a source terminal and a gate terminal. The drain terminal of the third switch transistor is coupled to the source terminal of the first switch transistor. The drain terminal of the fourth switch transistor is coupled to the source terminal of the second switch transistor. The first resistive memory element is coupled to the source terminal of the fourth switch transistor and the source terminal of the first switch transistor. The second resistive memory element is coupled to the source terminal of the third switch transistor and the source terminal of the second switch transistor.

Figure 1