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ACTIVE MATRIX DISPLAY DEVICE

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to an active matrix display device, more particularly to technology for eliminating band defect on the side ends of the screen of an active matrix display device driven by dot sequential scanning.

Description of Related Art

A typical schematic structure of a conventional active matrix display device is described briefly referring to Fig. 8. The active matrix display device has a plurality of gate lines X provided horizontally in parallel, a plurality of data lines Y provided vertically in parallel, and a plurality of picture elements PXL provided at each intersection of both the lines. The picture element comprises, for example, a small liquid crystal cell, and is provided so as to form a matrix which constitutes the display region. Thin film transistors Tr are integrated corresponding to each picture element PXL to drive the picture element. The device is provided with a vertical

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scanning circuit 101 which vertically scans each gate line X sequentially and selects picture elements PXL on one horizontal line every one horizontal period. The device is provided also with a horizontal scanning circuit 102 which scans each data line Y sequentially in one horizontal period to sample image signal Vsig, and writes by dot sequential scanning the image signal Vsig on picture elements on selected one horizontal line. In detail, each data line Y is connected to the video line 103 through horizontal switch HSW, and is supplied with image signal Vsig from the outside. The horizontal scanning circuit 102 outputs sampling pulses ϕ_{H1}, ϕ_{H2}, ϕ_{H3},... ϕ_{HN} sequentially to make and break each horizontal switch HSW and sample image signal Vsig on each data line Y.

Fig. 9 shows waveform of sampling pulses supplied sequentially from the horizontal scanning circuit 102 shown in Fig. 8. Sampling pulse duration τ_H is determined corresponding to sampling period assigned to each data line Y. Number of picture element has been increased to cause shortening of writing time per one dot as an active matrix display device has been refined. For an active matrix display device for HDTV, writing time per one dot is shortened due to speed up of line

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scanning. Correspondingly sampling pulse duration τ_H is inevitably shortened extremely. For example, in the case of a half-line active matrix display device with 470 horizontal picture elements for NTSC, sampling pulse duration is of the order of τ_H = 50•μs/470/3(RGB) = 320 ns. In the case of 800 horizontal picture elements, τ_H = 188 ns. Furthermore for doubled driving speed of full line system, sampling pulse duration τ_H is shortened to 94 ns. Shortening of sampling pulse duration causes the difficulty in wave shaping to result in use of complex horizontal scanning circuit structure of horizontal circuit and narrowed design option. Insufficient writing time causes the limitation on selectable design option of liquid crystal panel.

For example, a method disclosed in Japanese Patent Publication No. 1989-37911 has been proposed to solve the shortening problem of sampling pulse duration τ_H. In this technique, pulse durations of sampling pulse ϕ_{H1}, ϕ_{H2}, ϕ_{H3}, ϕ_{H4} ... are made longer and overlapped sampling pulses are output sequentially as illustrated in Fig. 10. This technique is a method in which a plurality of data lines are being selected simultaneously and the selected lines are being shifted sequentially. For example, in the case that four data

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lines are selected simultaneously as shown in Fig. 10, sampling pulse duration for 800 horizontal picture elements is of the order of τ_H = 4×188 ns = 750 ns. By applying this technique, the design limitation on the driving of the horizontal scanning circuit and also the design limitation on liquid crystal panel are reduced.

However, this method, in which a plurality of data lines are selected simultaneously and the group of selected data line is shifted sequentially, is involved disadvantageously in band defect on the side end in horizontal scanning direction on the display region 104 which constitutes the screen as shown in Fig. 11. For example when the display is in normal white mode, the band defect 105 appears as a band darker than normal region. The band defect 105 is attributed to the release of sampling pulses from overlapping at the side end of horizontal scanning and to driving condition different from that of normal region.

OBJECTS AND SUMMARY OF THE INVENTION

It is the object of the present invention to eliminate the band defect on the side end of horizontal scanning in the dot sequential driving of an active matrix display device. The band defect is a

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disadvantage of the above-mentioned technique. To attain the object, a technique described hereinafter has been created. An active matrix display device of the invention has three basic components of a plurality of gate lines provided horizontally in parallel, a plurality of data lines provided vertically in parallel, and a plurality of picture elements provided at each intersection of both lines which picture elements constitute the display region, In addition, the display device is provided with a vertical scanning circuit and horizontal scanning circuit as peripheral component. The vertical scanning circuit scans vertically each gate line sequentially to select picture elements on one horizontal line every horizontal period. On the other hand, the horizontal scanning circuit scans each data line sequentially to sample image signals in one horizontal period, and writes by dot sequential scanning the image signals on picture elements on selected one horizontal line. The data lines of the present invention are defined characteristically into two sections, that is real data lines provided in the display region and additional dummy data lines provided outside the display region which dummy lines intersect with the end sections of gate lines. The horizontal

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scanning circuit scans horizontally the real data lines with a sampling timing so as that a plurality of pulses overlaps, and subsequently the horizontal scanning circuit scans additionally the dummy data lines with the sampling timing in the same manner as scanned on the data lines. In this case, it is required that at least so many dummy data lines as horizontally scanned simultaneously with a certain overlapped sampling timing are provided.

According to the present invention, dummy data lines are provided additionally outside the display region adjacent to the ends of real data lines provided in the display region. The horizontal scanning circuit scans horizontally real data lines and then dummy data lines continuously. At the side end of the display region, the overlapped sampling timing on a plurality of real data lines is maintained, therefore image display is normal at the side end and no band defect is displayed. When horizontal scanning reaches dummy data lines, overlapped sampling timing is released and quality of displaying can change depending on the case. However, it does not make the problem because dummy data lines are provided outside the display region, and band defect will not appear on the display.

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BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a circuit diagram for illustrating the structure of an active matrix display device in accordance with the present invention.

Fig. 2 is a timing chart for operational description of the active matrix display device shown in Fig. 1.

Fig. 3 is a reference circuit diagram for description of band defect.

Fig. 4 is a timing chart.

Fig. 5 is a reference equivalent circuit diagram.

Fig. 6 is a reference timing chart.

Fig. 7 is a reference graph.

Fig. 8 is a circuit diagram for illustrating typical structure of a conventional active matrix display device.

Fig. 9 is a timing chart for operational description of the active matrix display device shown in Fig. 8.

Fig. 10 is a timing chart for operational description.

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Fig. 11 is a schematic diagram for illustrating band defect on the display region.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A preferable embodiment of the invention will be described in detail referring to the drawings. Fig. 1 is a circuit diagram for illustration of an embodiment of an active matrix display device of the invention. As shown in the figure, the active matrix display device has a plurality of gate line X provided horizontally in parallel and a plurality of data lines Y provided vertically in parallel. Picture elements PXL are provided at intersections of both lines to form a matrix, and the picture elements constitute the display region 1. The picture elements PXL comprise liquid crystal cells with fine structure. In this embodiment, thin film transistors Tr are provided to drive picture elements PXL comprising liquid crystal cells. Source electrodes of thin film transistors Tr are connected individually to corresponding data line Y, gate electrodes are connected to corresponding gate lines X, and drain electrodes are connected to corresponding picture elements PXL.

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A vertical scanning circuit 2 and horizontal scanning circuit 3 are provided around the display region 1. The vertical scanning circuit 2 scans vertically each gate line Y sequentially to make thin film transistors conductive, and picture elements PXL on one horizontal line are selected every one horizontal period. On the other hand, the horizontal scanning circuit 3 scans each data line Y sequentially in one horizontal period to sample image signal Vsig and writes by dot sequential scanning the image signal Vsig on picture elements PXL on selected one horizontal line. In detail, each data line Y is connected to the video line 4 through horizontal switches HSW and receives the supply of image signal Vsig. The horizontal scanning circuit 3 outputs sampling pulses ϕ and inverted pulses sequentially to make and break controllably the horizontal switch HSW and the above-mentioned image signal Vsig are sampled. Image signal Vsig sampled on each data lines Y are written on picture elements PXL on one horizontal line through thin film transistors Tr which is on. Afterwards, the thin film transistors Tr are switched off, and written image signals Vsig are retained until next frame.

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It is the characteristics of this invention that data lines are defined into two sections of real data lines Y1, Y2, ..., YL provided in the display region 1 and dummy data lines YD1, YD2, YD3, and YD4 provided outside the display region 1. These dummy lines intersects with the end sections of gate lines X. In this embodiment, picture elements PXL and thin film transistors Tr are removed from the dummy data lines. The present invention is not limited to this embodiment, dummy picture elements and thin film transistors may assigned to the dummy data lines for complete unification of the driving condition. On the other hand, the horizontal scanning circuit 3 scans not only the real data lines but also the dummy data lines. The horizontal scanning circuit 3 horizontally scans on the real data lines Y1, Y2,...,YL with a sampling timing overlapping a plurality of data lines (in this embodiment, four lines). Subsequently, the horizontal scanning circuit 3 horizontally scans additionally the dummy data lines YD1, YD2, YD3, and YD4 with the same overlapped sampling timing as scanned on the real data lines. In this case, it is required that at least so many the dummy data lines as horizontally scanned simultaneously with a certain overlapped sampling timing

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are provided. In this embodiment at least four dummy data lines are provided. The dummy data line are described in detail herein under. The horizontal scanning circuit 3 outputs sampling pulses $\phi 1$, $\phi 2$, ... ϕL and inverted pulses sequentially on horizontal switches HSW connected to the real data lines Y1, Y2, ...,YL. Subsequently, the horizontal scanning circuit 3 outputs sampling pulses $\phi D1$, $\phi D2$, $\phi D3$, $\phi D4$ and inverted pulses sequentially on horizontal switches HSW connected to the dummy data lines YD1, YD2, YD3, and YD4. In this embodiment, inverted pulses are output because transmission gates comprising CMOS are used as the horizontal switch HSW.

Operation of the active matrix display device illustrated in Fig. 1 is described in detail referring to Fig. 2. As shown in the timing chart in Fig. 2, sampling pulses are output on the real data lines with a sampling timing overlapping four lines to scan horizontally the display region 1 (real scanning). For easy understanding of the timing chart, five real sampling pulses from the first pulse to the final pulse ϕL are shown. In this embodiment, the rising of a sampling pulse ϕL is followed by successive output of dummy sampling pulses $\phi D1$, $\phi D2$, $\phi D3$, $\phi D4$ with the same

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overlapped sampling timing on dummy data lines to scan horizontally outside the display region (dummy scanning). Output of successive sampling pulses ϕ with overlapped timing as described herein above generates the voltage swinging of gate lines Y due to capacity coupling at intersections of gate lines Y and data lines X. Corresponding to each rising of sampling pulse ϕ, gate lines receive sequentially capacity coupling, consequently voltage of gate lines X continue to swing until final dummy sampling pulse ϕD4 rises. After the rise of final dummy sampling pulse ϕD4, voltage of gate lines Y decays gradually toward the ground level because gate lines receive no longer capacity coupling.

On the other hand, when each sampling pulse ϕ rises, horizontal switches HSW are changed from on to off. Closed HSW causes jumping of the voltage swinging of gate lines to each signal lines Y. As the result, when voltage of gate lines start to decay after cease of swinging, the decay affects on the voltage of signal line X through capacity coupling to cause decay. As understood from the timing chart in Fig. 2, voltages of real data lines V_{L-4}, V_{L-3}, V_{L-3}, V_{L-1}, and V_L start to decay all at once after swinging of gate lines ceased, because corresponding HSW is already off, and the decay

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finally causes voltage drop of ΔV0. The voltage drop ΔV0 are identical for all the real data lines, consequently there appears no dark band display. On the other hand, for example for the first dummy data line YD1, after cease of voltage swinging, the corresponding dummy sampling pulse ϕD1 falls with delay of one clock period. Because voltage VD1 starts to decay synchronously with the falling, final voltage drop ΔV1 is smaller than ΔV0. Similarly, for the second dummy data line YD2, because VD2 starts to decay with delay of one more clock period, final voltage drop ΔV2 is smaller than ΔV1. As mentioned above, voltage drops of the dummy data lines are different each other, and the difference results in fluctuated display brightness. However, the dummy data lines are provided outside the display region 1, therefore the fluctuation does not affect on an actual image on the display. As described above, the horizontal scanning circuit 3 scans horizontally extra four picture elements in addition to the effective display region 1. Four dummy data lines including HSW are provided on the area outside the display region 1 in the same arrangement as provided in the display region 1. By providing the four dummy data lines, swinging of gate lines continues similarly from

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the effective display region 1 to the outside area covering four picture elements. Consequently, swinging of signal lines included in the display region 1 is limited to the side end, and does not change rapidly. In this embodiment, four signal lines are horizontally scanned simultaneously, and generally in the case of simultaneous scanning on n signal lines, at least n dummy data lines are required. Picture element and transistor for driving are not necessarily required, and the band effect elimination effect is sufficient without picture element and transistor for driving.

Finally, the mechanism of band defect generation is described for better understanding referring to Fig. 3 to Fig. 7. Fig. 3 shows the structure of a typical active matrix display device, and is the same device as shown in Fig. 8. On the corresponding components, corresponding same numerals are indicated for easy understanding. Reference symbols which are used in the following description are described. The voltage of video line 103 supplied with image signal Vsig is represented by VA. Voltage of individual data lines Y is represented by VB. Voltage of each gate line X is represented by VC. Parasitic capacity Ch interposes at the intersections of each gate

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line X and data line Y, and the parasitic capacity Ch causes the above-mentioned capacity coupling. Resistance component is included in each gate line X.

Fig. 4 illustrates voltage VA, Vb, and VC change of each line with time. As illustrated, a sampling pulse ϕ_H is output from the horizontal scanning circuit 102, and image signal Vsig is sample-held on the corresponding data line. Voltage VB of sample-held data line and Voltage VC of gate line are apparently flat, but the enlarging of VB and VC around the sampling timing reveals fluctuation due to the above-mentioned capacity coupling. Signals of differential waveform are superposed continuously on the gate voltage VC. Data voltage VB decays from the sample-hold level.

Fig. 5 shows a circuit equivalent with this part. Individual data lines intersect with all gate lines behind corresponding HSW. Therefore, the equivalent circuit includes a capacity C_H equivalent with the total parasitic capacity shown in Fig. 3. C_G in the equivalent circuit represents the total capacity of the gate lines itself, and R_G represents the equivalent gate line resistance. In this circuit, when data voltage VB rises, gate voltage VC also rises correspondingly. When HSW is closed, decay of the gate

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voltage VC is reflected on the data voltage VB analogously.

Corresponding behavior of the simultaneous four line scanning is illustrated referring to the timing chart in Fig. 6. For easy description, five sampling pulses from the final sampling pulse $\phi_{H,LAST}$ to $\phi_{H,LAST-4}$ are shown. Charge and discharge to signal lines are repeated until the final sampling pulse ϕH,LAST rises. Due to the repeated charge and discharge, gate voltage VC receives sequentially capacity coupling at each ϕ_H rise. After the rise of $\phi_{H,LAST}$, the gate voltage VC decays toward the ground level because the gate voltage VC no longer receive capacity coupling. On the other hand, after closing of corresponding HSW, swinging of the gate voltage jumps to each signal line through the capacity component C_H of the equivalent circuit illustrated in Fig. 5.

Before the timing of $\phi_{H,LAST-4}$, the level of signal line changes by ΔV0 as shown on the VBLAST-4. The level of jumping to signal line due to gate voltage VC decay decreases step by step with shifting from $\phi_{H,Last-3}$, to $\phi_{H,LST-2}$, and $\phi_{H,LST-1}$, ... Voltage drop ΔV1, ... ΔV4 for the final four signal line voltages

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VB_{LAST-3}, ..., VB_{LAST} decreases in the order from LAST-3 to LAST.

The ΔV is illustrated schematically in Fig. 7. ΔV of the final four signal lines is smaller than that of all previous signal lines. The decrement increases as the signal line approaches to the final signal line. Accordingly, the band defect is resulted on the final four lines.

As described hereinbefore, according to the present invention, dummy data lines are provided outside the display region in addition to real data lines provided in the display region. The real data lines are scanned horizontally with a sampling timing overlapping on a plurality of data lines, and then additionally the dummy data lines are scanned horizontally with the same sampling timing as scanned on the real data lines, thereby the band defect is eliminated and image quality is improved. Especially, this invention is effective for large size active matrix display devices which utilize increased number of picture elements with dot sequence drive.

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What Is Claimed Is:

1. An active matrix display device comprising:

a plurality of gate lines provided on horizontal lines,

a plurality of data lines provided vertically,

a plurality of picture elements provided at each intersection of said gate lines and data lines which constitute the display region,

a vertical scanning circuit for scanning vertically each gate line sequentially to select picture elements for each horizontal line, and

a horizontal scanning circuit to sample image signals and subsequently write the image signals on picture elements on a selected horizontal line by dot sequential scanning, wherein

said data lines are defined to two sections of real data lines provided in said display region and dummy data lines provided outside said display region which dummy data line intersect with the end section of the gate lines, and

said horizontal canning circuit operates the first scanning horizontally on said real data lines

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with a sampling timing overlapping a plurality of real data lines, and, subsequently to said first scanning, operates the second scanning horizontally also on said dummy data lines with the overlapped sampling timing.

2. An active matrix display device as claimed in claim 1, wherein at least so many said dummy data lines as horizontally scanned simultaneously with a certain overlapped sampling timing are provided.

3. An active matrix display device as claimed in claim 1, wherein dummy picture elements corresponding to said dummy data lines are provided.

4. An active matrix display device as claimed in claim 1, wherein picture elements are provided on only said data lines.

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ABSTRACT OF THE DISCLOSURE

ACTIVE MATRIX DISPLAY DEVICE

The active matrix display device has a plurality of gate lines Y provided on horizontal lines, a plurality of data lines X provided on vertical lines, and a plurality of picture elements provided at each intersection of both lines. The picture elements PXL provided horizontally constitute the display region 1. The vertical scanning circuit 2 scans vertically each gate line X sequentially, and selects picture elements on one horizontal line every one horizontal period. The horizontal scanning circuit 3 scans each data line Y sequentially in one horizontal period, samples image signal Vsig, and writes by dot sequential scanning the image signal Vsig on picture elements PXL on selected one horizontal line. The data lines are defined to two sections of real data lines Y1, Y2, ...,YL provided in the display region 1 and dummy data lines YD1, YD2, YD3, and YD4 provided outside the display region which dummy data lines intersect with the end section of the data lines. The horizontal scanning circuit 3 scans horizontally on the real data lines Y1, Y2,...,YL with a sampling timing overlapping a plurality of the real data lines, subsequently continue to scan on the dummy data

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lines YD1, YD2, YD3 and YD4 with the overlapped sampling timing.

Thereby band defect on the side end of the screen when an active matrix display device is driven dot sequentially is eliminated.

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FIG. 1

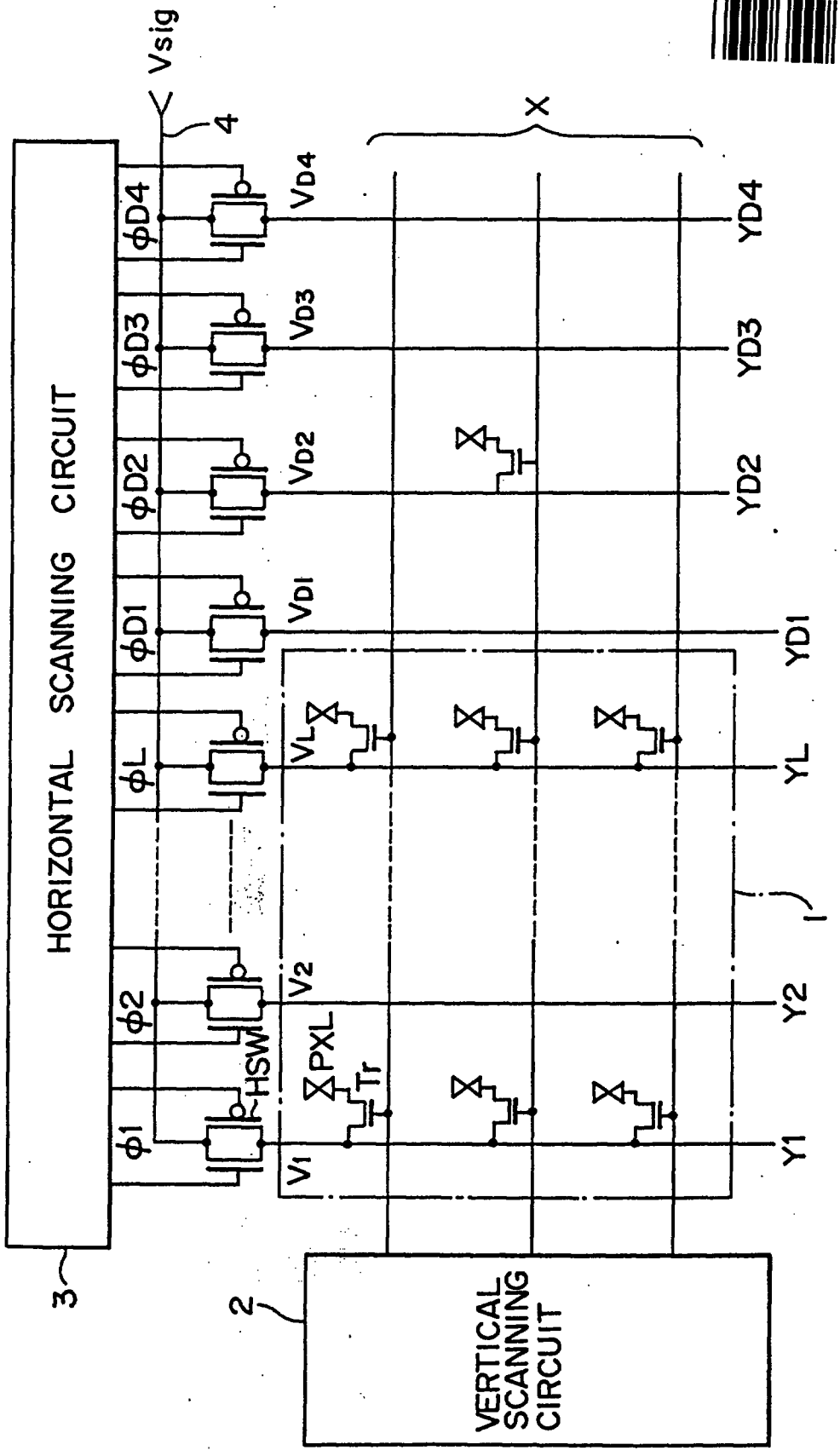

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FIG. 2

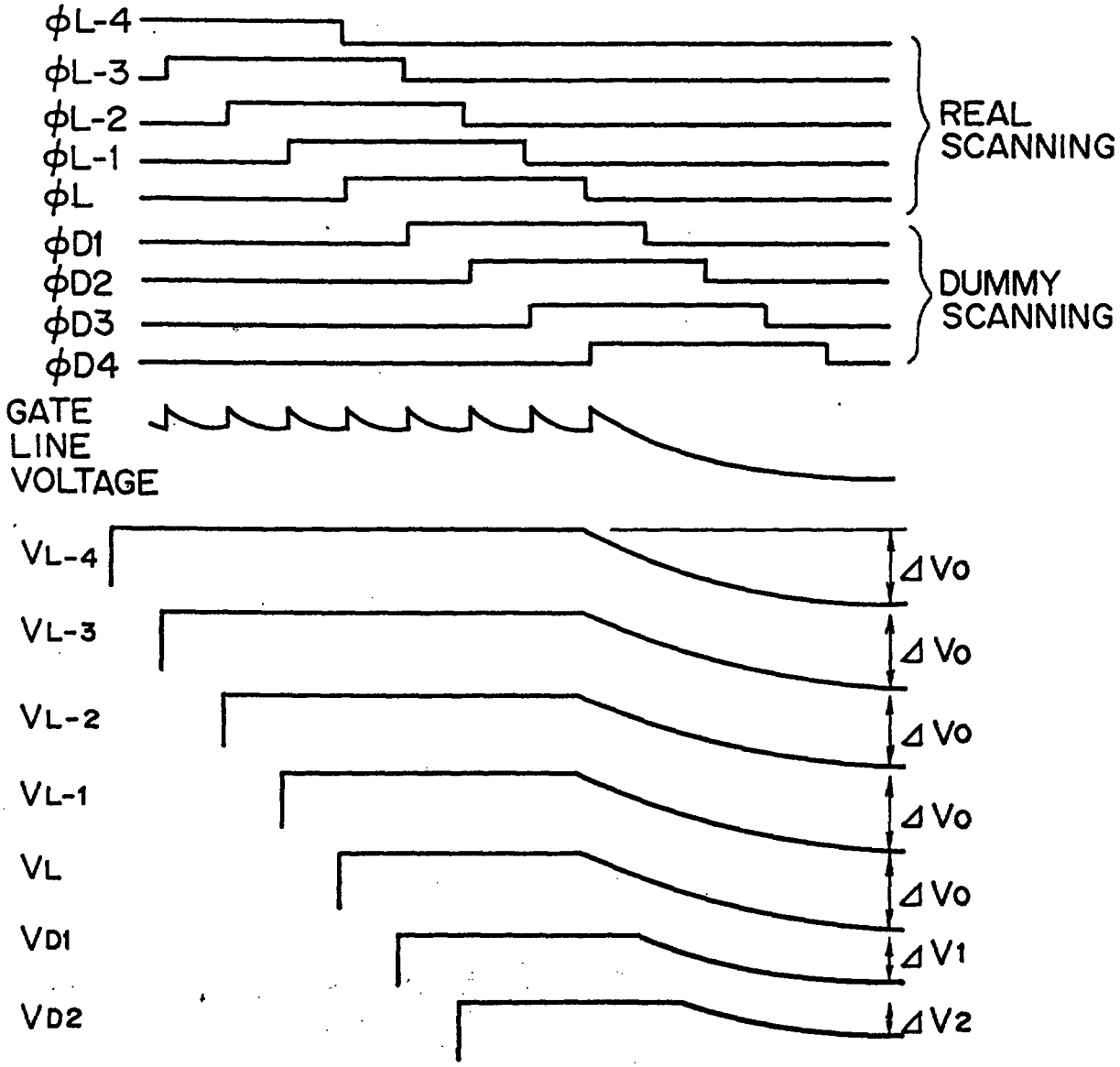

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FIG. 3

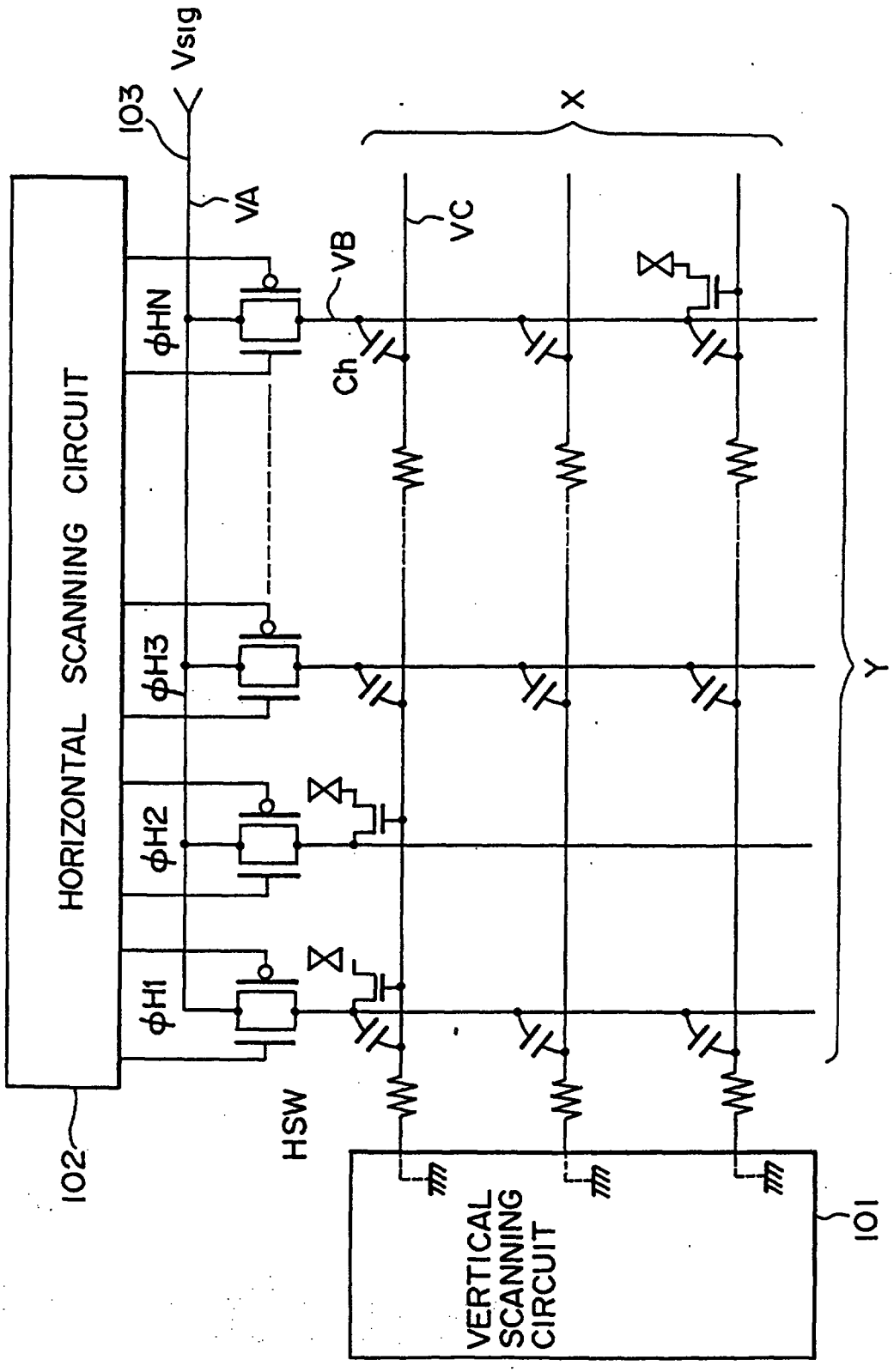

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FIG. 4

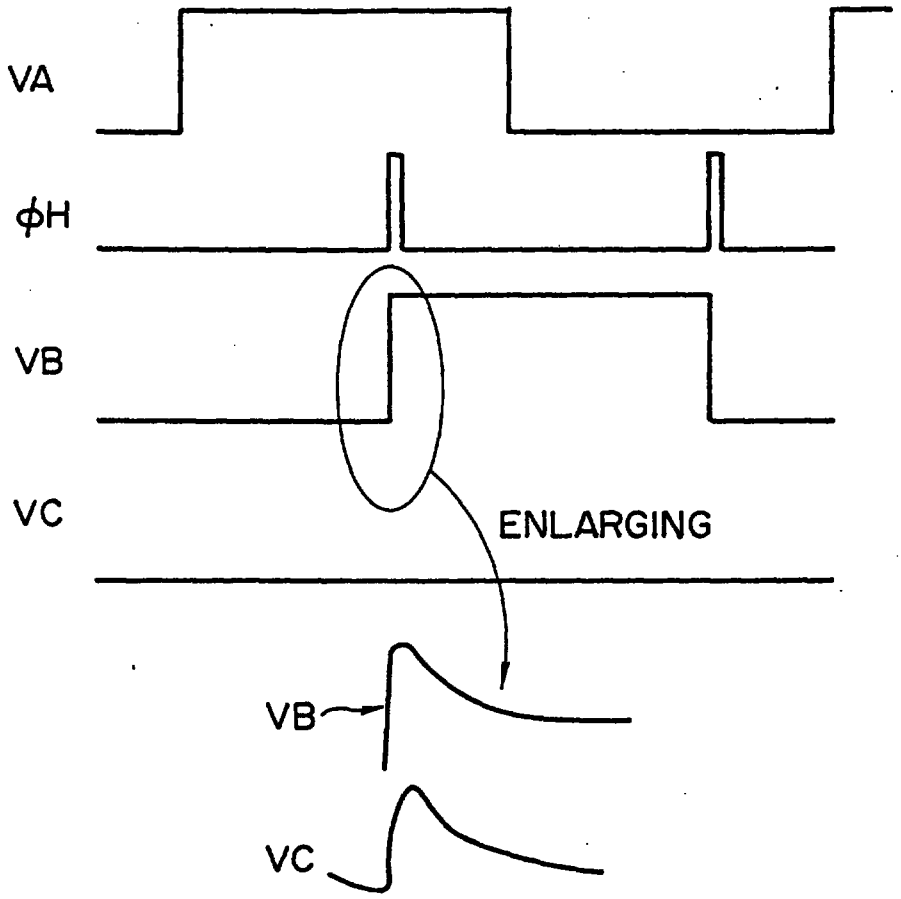

FIG. 5

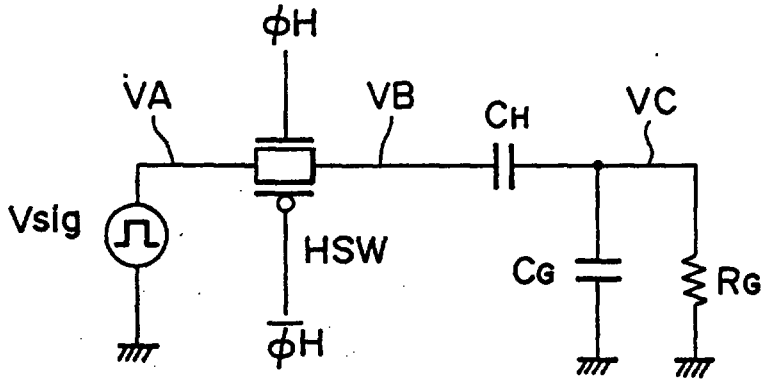

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FIG. 6

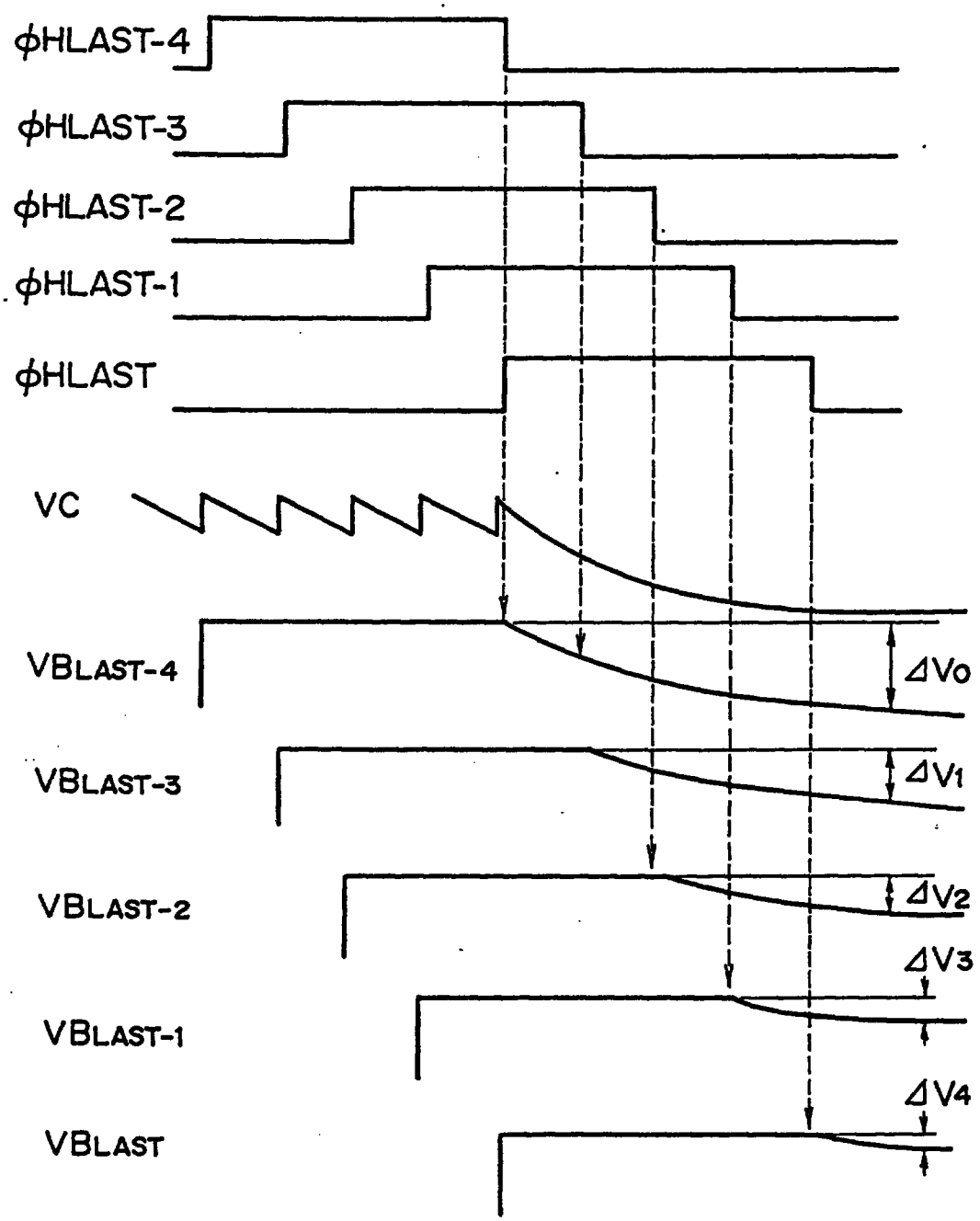

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FIG. 7

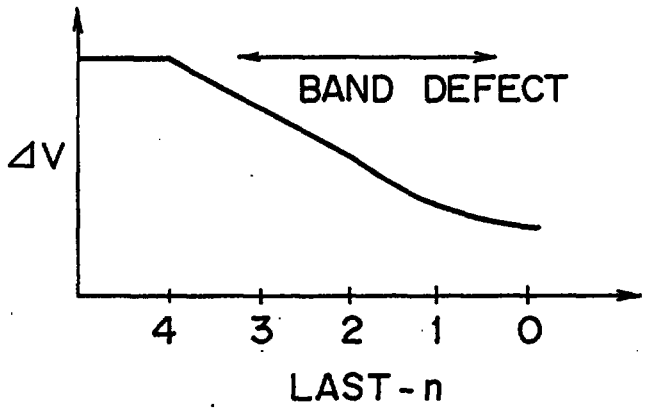

FIG. 8

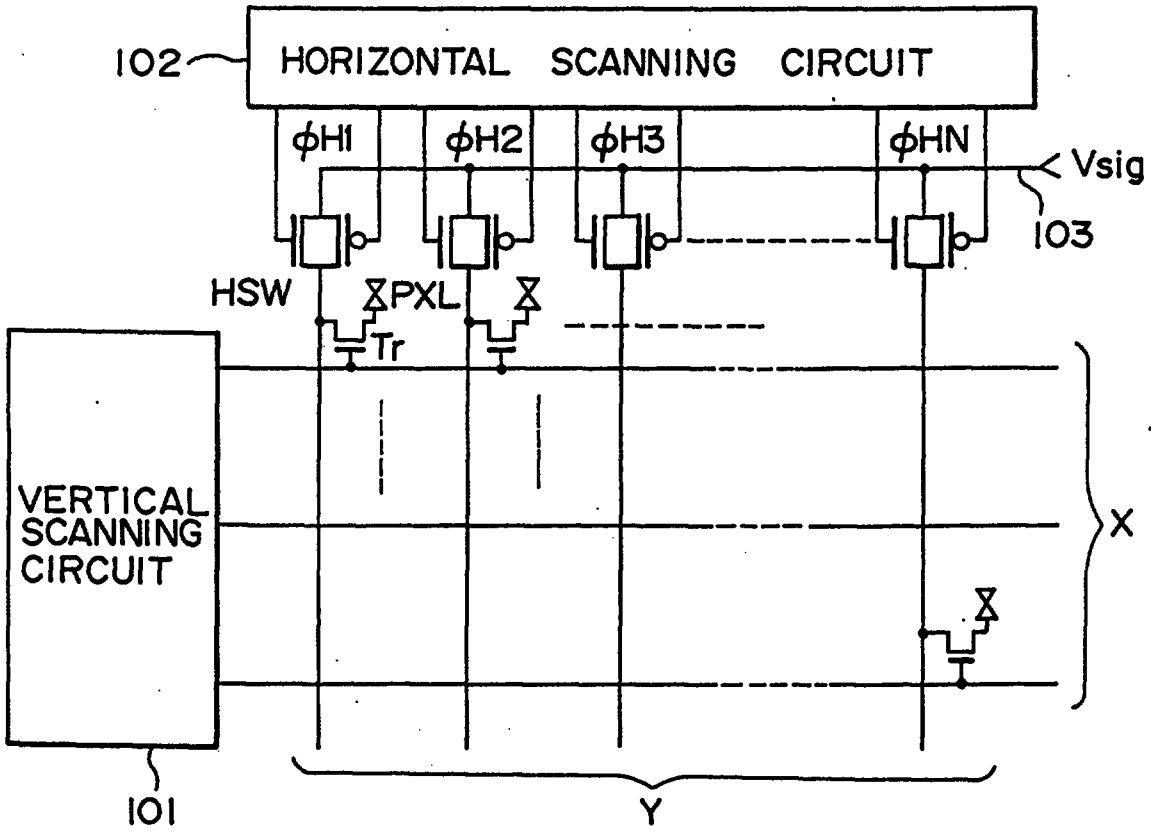

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FIG. 9

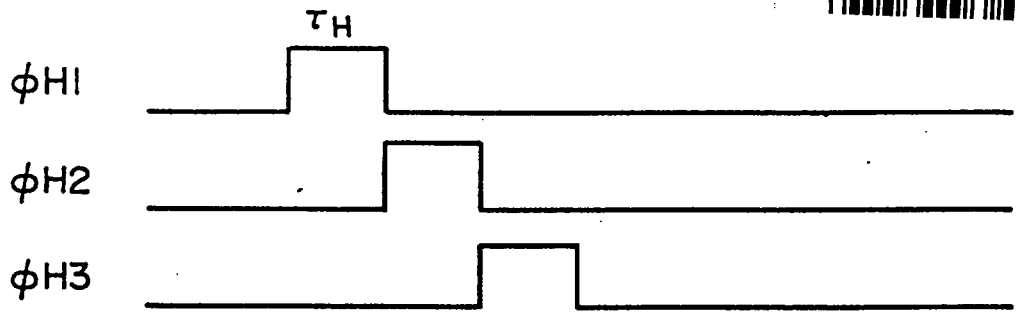


FIG. 10

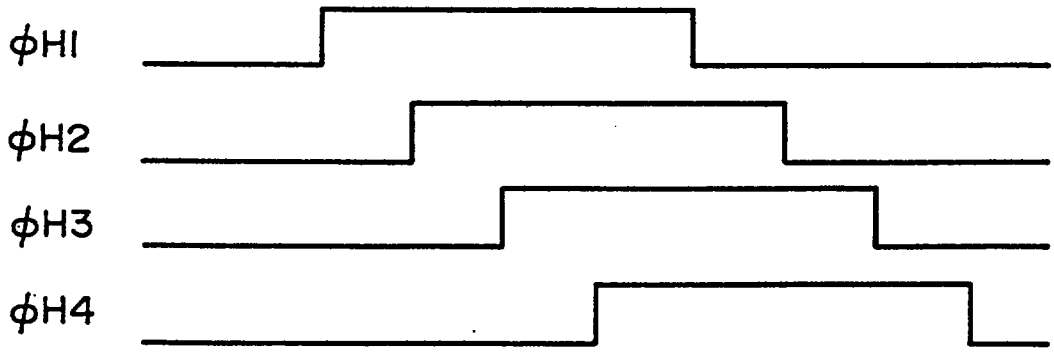
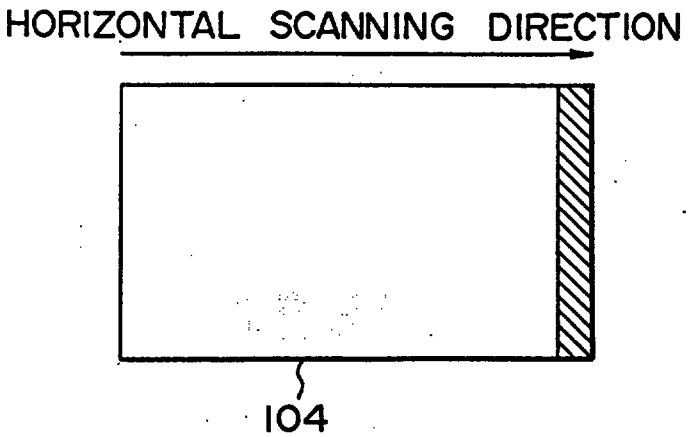


FIG. 11



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ACTIVE MATRIX DISPLAY DEVICE

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to an active matrix display device, more particularly to technology for eliminating band defect on the side ends of the screen of an active matrix display device driven by dot sequential scanning.

Description of Related Art

A typical schematic structure of a conventional active matrix display device is described briefly referring to Fig. 8. The active matrix display device has a plurality of gate lines X provided horizontally in parallel, a plurality of data lines Y provided vertically in parallel, and a plurality of picture elements PXL provided at each intersection of both the lines. The picture element comprises, for example, a small liquid crystal cell, and is provided so as to form a matrix which constitutes the display region. Thin film transistors Tr are integrated corresponding to each picture element PXL to drive the picture element. The device is provided with a vertical

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scanning circuit 101 which vertically scans each gate line X sequentially and selects picture elements PXL on one horizontal line every one horizontal period. The device is provided also with a horizontal scanning circuit 102 which scans each data line Y sequentially in one horizontal period to sample image signal Vsig, and writes by dot sequential scanning the image signal Vsig on picture elements on selected one horizontal line. In detail, each data line Y is connected to the video line 103 through horizontal switch HSW, and is supplied with image signal Vsig from the outside. The horizontal scanning circuit 102 outputs sampling pulses ϕ_{H1}, ϕ_{H2}, ϕ_{H3},... ϕ_{HN} sequentially to make and break each horizontal switch HSW and sample image signal Vsig on each data line Y.

Fig. 9 shows waveform of sampling pulses supplied sequentially from the horizontal scanning circuit 102 shown in Fig. 8. Sampling pulse duration τ_H is determined corresponding to sampling period assigned to each data line Y. Number of picture element has been increased to cause shortening of writing time per one dot as an active matrix display device has been refined. For an active matrix display device for HDTV, writing time per one dot is shortened due to speed up of line

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scanning. Correspondingly sampling pulse duration τ_H is inevitably shortened extremely. For example, in the case of a half-line active matrix display device with 470 horizontal picture elements for NTSC, sampling pulse duration is of the order of τ_H = 50 μs/470/3(RGB) = 320 ns. In the case of 800 horizontal picture elements, τ_H = 188 ns. Furthermore for doubled driving speed of full line system, sampling pulse duration τ_H is shortened to 94 ns. Shortening of sampling pulse duration causes the difficulty in wave shaping to result in use of complex horizontal scanning circuit structure of horizontal circuit and narrowed design option. Insufficient writing time causes the limitation on selectable design option of liquid crystal panel.

For example, a method disclosed in Japanese Patent Publication No. 1989-37911 has been proposed to solve the shortening problem of sampling pulse duration τ_H. In this technique, pulse durations of sampling pulse ϕ_{H1}, ϕ_{H2}, ϕ_{H3}, ϕ_{H4} ... are made longer and overlapped sampling pulses are output sequentially as illustrated in Fig. 10. This technique is a method in which a plurality of data lines are being selected simultaneously and the selected lines are being shifted sequentially. For example, in the case that four data

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lines are selected simultaneously as shown in Fig. 10, sampling pulse duration for 800 horizontal picture elements is of the order of τ_H = 4×188 ns = 750 ns. By applying this technique, the design limitation on the driving of the horizontal scanning circuit and also the design limitation on liquid crystal panel are reduced.

However, this method, in which a plurality of data lines are selected simultaneously and the group of selected data line is shifted sequentially, is involved disadvantageously in band defect on the side end in horizontal scanning direction on the display region 104 which constitutes the screen as shown in Fig. 11. For example when the display is in normal white mode, the band defect 105 appears as a band darker than normal region. The band defect 105 is attributed to the release of sampling pulses from overlapping at the side end of horizontal scanning and to driving condition different from that of normal region.

OBJECTS AND SUMMARY OF THE INVENTION

It is the object of the present invention to eliminate the band defect on the side end of horizontal scanning in the dot sequential driving of an active matrix display device. The band defect is a

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disadvantage of the above-mentioned technique. To attain the object, a technique described hereinafter has been created. An active matrix display device of the invention has three basic components of a plurality of gate lines provided horizontally in parallel, a plurality of data lines provided vertically in parallel, and a plurality of picture elements provided at each intersection of both lines which picture elements constitute the display region, In addition, the display device is provided with a vertical scanning circuit and horizontal scanning circuit as peripheral component. The vertical scanning circuit scans vertically each gate line sequentially to select picture elements on one horizontal line every horizontal period. On the other hand, the horizontal scanning circuit scans each data line sequentially to sample image signals in one horizontal period, and writes by dot sequential scanning the image signals on picture elements on selected one horizontal line. The data lines of the present invention are defined characteristically into two sections, that is real data lines provided in the display region and additional dummy data lines provided outside the display region which dummy lines intersect with the end sections of gate lines. The horizontal

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scanning circuit scans horizontally the real data lines with a sampling timing so as that a plurality of pulses overlaps, and subsequently the horizontal scanning circuit scans additionally the dummy data lines with the sampling timing in the same manner as scanned on the data lines. In this case, it is required that at least so many dummy data lines as horizontally scanned simultaneously with a certain overlapped sampling timing are provided.

According to the present invention, dummy data lines are provided additionally outside the display region adjacent to the ends of real data lines provided in the display region. The horizontal scanning circuit scans horizontally real data lines and then dummy data lines continuously. At the side end of the display region, the overlapped sampling timing on a plurality of real data lines is maintained, therefore image display is normal at the side end and no band defect is displayed. When horizontal scanning reaches dummy data lines, overlapped sampling timing is released and quality of displaying can change depending on the case. However, it does not make the problem because dummy data lines are provided outside the display region, and band defect will not appear on the display.

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BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a circuit diagram for illustrating the structure of an active matrix display device in accordance with the present invention.

Fig. 2 is a timing chart for operational description of the active matrix display device shown in Fig. 1.

Fig. 3 is a reference circuit diagram for description of band defect.

Fig. 4 is a timing chart.

Fig. 5 is a reference equivalent circuit diagram.

Fig. 6 is a reference timing chart.

Fig. 7 is a reference graph.

Fig. 8 is a circuit diagram for illustrating typical structure of a conventional active matrix display device.

Fig. 9 is a timing chart for operational description of the active matrix display device shown in Fig. 8.

Fig. 10 is a timing chart for operational description.

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Fig. 11 is a schematic diagram for illustrating band defect on the display region.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A preferable embodiment of the invention will be described in detail referring to the drawings. Fig. 1 is a circuit diagram for illustration of an embodiment of an active matrix display device of the invention. As shown in the figure, the active matrix display device has a plurality of gate line X provided horizontally in parallel and a plurality of data lines Y provided vertically in parallel. Picture elements PXL are provided at intersections of both lines to form a matrix, and the picture elements constitute the display region 1. The picture elements PXL comprise liquid crystal cells with fine structure. In this embodiment, thin film transistors Tr are provided to drive picture elements PXL comprising liquid crystal cells. Source electrodes of thin film transistors Tr are connected individually to corresponding data line Y, gate electrodes are connected to corresponding gate lines X, and drain electrodes are connected to corresponding picture elements PXL.

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A vertical scanning circuit 2 and horizontal scanning circuit 3 are provided around the display region 1. The vertical scanning circuit 2 scans vertically each gate line Y sequentially to make thin film transistors conductive, and picture elements PXL on one horizontal line are selected every one horizontal period. On the other hand, the horizontal scanning circuit 3 scans each data line Y sequentially in one horizontal period to sample image signal Vsig and writes by dot sequential scanning the image signal Vsig on picture elements PXL on selected one horizontal line. In detail, each data line Y is connected to the video line 4 through horizontal switches HSW and receives the supply of image signal Vsig. The horizontal scanning circuit 3 outputs sampling pulses ϕ and inverted pulses sequentially to make and break controllably the horizontal switch HSW and the above-mentioned image signal Vsig are sampled. Image signal Vsig sampled on each data lines Y are written on picture elements PXL on one horizontal line through thin film transistors Tr which is on. Afterwards, the thin film transistors Tr are switched off, and written image signals Vsig are retained until next frame.

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It is the characteristics of this invention that data lines are defined into two sections of real data lines Y1, Y2, ..., YL provided in the display region 1 and dummy data lines YD1, YD2, YD3, and YD4 provided outside the display region 1. These dummy lines intersects with the end sections of gate lines X. In this embodiment, picture elements PXL and thin film transistors Tr are removed from the dummy data lines. The present invention is not limited to this embodiment, dummy picture elements and thin film transistors may assigned to the dummy data lines for complete unification of the driving condition. On the other hand, the horizontal scanning circuit 3 scans not only the real data lines but also the dummy data lines. The horizontal scanning circuit 3 horizontally scans on the real data lines Y1, Y2,...,YL with a sampling timing overlapping a plurality of data lines (in this embodiment, four lines). Subsequently, the horizontal scanning circuit 3 horizontally scans additionally the dummy data lines YD1, YD2, YD3, and YD4 with the same overlapped sampling timing as scanned on the real data lines. In this case, it is required that at least so many the dummy data lines as horizontally scanned simultaneously with a certain overlapped sampling timing

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are provided. In this embodiment at least four dummy data lines are provided. The dummy data line are described in detail herein under. The horizontal scanning circuit 3 outputs sampling pulses ϕ1, ϕ2, ... ϕL and inverted pulses sequentially on horizontal switches HSW connected to the real data lines Y1, Y2, ...,YL. Subsequently, the horizontal scanning circuit 3 outputs sampling pulses ϕD1, ϕD2, ϕD3, ϕD4 and inverted pulses sequentially on horizontal switches HSW connected to the dummy data lines YD1, YD2, YD3, and YD4. In this embodiment, inverted pulses are output because transmission gates comprising CMOS are used as the horizontal switch HSW.

Operation of the active matrix display device illustrated in Fig. 1 is described in detail referring to Fig. 2. As shown in the timing chart in Fig. 2, sampling pulses are output on the real data lines with a sampling timing overlapping four lines to scan horizontally the display region 1 (real scanning). For easy understanding of the timing chart, five real sampling pulses from the first pulse to the final pulse ϕL are shown. In this embodiment, the rising of a sampling pulse ϕL is followed by successive output of dummy sampling pulses ϕD1, ϕD2, ϕD3, ϕD4 with the same

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overlapped sampling timing on dummy data lines to scan horizontally outside the display region (dummy scanning). Output of successive sampling pulses ϕ with overlapped timing as described herein above generates the voltage swinging of gate lines Y due to capacity coupling at intersections of gate lines Y and data lines X. Corresponding to each rising of sampling pulse ϕ, gate lines receive sequentially capacity coupling, consequently voltage of gate lines X continue to swing until final dummy sampling pulse ϕD4 rises. After the rise of final dummy sampling pulse ϕD4, voltage of gate lines Y decays gradually toward the ground level because gate lines receive no longer capacity coupling.

On the other hand, when each sampling pulse ϕ rises, horizontal switches HSW are changed from on to off. Closed HSW causes jumping of the voltage swinging of gate lines to each signal lines Y. As the result, when voltage of gate lines start to decay after cease of swinging, the decay affects on the voltage of signal line X through capacity coupling to cause decay. As understood from the timing chart in Fig. 2, voltages of real data lines V_{L-4}, V_{L-3}, V_{L-3}, V_{L-1}, and V_L start to decay all at once after swinging of gate lines ceased, because corresponding HSW is already off, and the decay

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finally causes voltage drop of ΔV0. The voltage drop ΔV0 are identical for all the real data lines, consequently there appears no dark band display. On the other hand, for example for the first dummy data line YD1, after cease of voltage swinging, the corresponding dummy sampling pulse ϕD1 falls with delay of one clock period. Because voltage VD1 starts to decay synchronously with the falling, final voltage drop ΔV1 is smaller than ΔV0. Similarly, for the second dummy data line YD2, because VD2 starts to decay with delay of one more clock period, final voltage drop ΔV2 is smaller than ΔV1. As mentioned above, voltage drops of the dummy data lines are different each other, and the difference results in fluctuated display brightness. However, the dummy data lines are provided outside the display region 1, therefore the fluctuation does not affect on an actual image on the display. As described above, the horizontal scanning circuit 3 scans horizontally extra four picture elements in addition to the effective display region 1. Four dummy data lines including HSW are provided on the area outside the display region 1 in the same arrangement as provided in the display region 1. By providing the four dummy data lines, swinging of gate lines continues similarly from

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the effective display region 1 to the outside area covering four picture elements. Consequently, swinging of signal lines included in the display region 1 is limited to the side end, and does not change rapidly. In this embodiment, four signal lines are horizontally scanned simultaneously, and generally in the case of simultaneous scanning on n signal lines, at least n dummy data lines are required. Picture element and transistor for driving are not necessarily required, and the band effect elimination effect is sufficient without picture element and transistor for driving.

Finally, the mechanism of band defect generation is described for better understanding referring to Fig. 3 to Fig. 7. Fig. 3 shows the structure of a typical active matrix display device, and is the same device as shown in Fig. 8. On the corresponding components, corresponding same numerals are indicated for easy understanding. Reference symbols which are used in the following description are described. The voltage of video line 103 supplied with image signal Vsig is represented by VA. Voltage of individual data lines Y is represented by VB. Voltage of each gate line X is represented by VC. Parasitic capacity Ch interposes at the intersections of each gate

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line X and data line Y, and the parasitic capacity Ch causes the above-mentioned capacity coupling. Resistance component is included in each gate line X.

Fig. 4 illustrates voltage VA, Vb, and VC change of each line with time. As illustrated, a sampling pulse ϕ_H is output from the horizontal scanning circuit 102, and image signal Vsig is sample-held on the corresponding data line. Voltage VB of sample-held data line and Voltage VC of gate line are apparently flat, but the enlarging of VB and VC around the sampling timing reveals fluctuation due to the above-mentioned capacity coupling. Signals of differential waveform are superposed continuously on the gate voltage VC. Data voltage VB decays from the sample-hold level.

Fig. 5 shows a circuit equivalent with this part. Individual data lines intersect with all gate lines behind corresponding HSW. Therefore, the equivalent circuit includes a capacity C_H equivalent with the total parasitic capacity shown in Fig. 3. C_G in the equivalent circuit represents the total capacity of the gate lines itself, and R_G represents the equivalent gate line resistance. In this circuit, when data voltage VB rises, gate voltage VC also rises correspondingly. When HSW is closed, decay of the gate

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voltage VC is reflected on the data voltage VB analogously.

Corresponding behavior of the simultaneous four line scanning is illustrated referring to the timing chart in Fig. 6. For easy description, five sampling pulses from the final sampling pulse $\phi_{H,LAST}$ to $\phi_{H,LAST-4}$ are shown. Charge and discharge to signal lines are repeated until the final sampling pulse ϕH,LAST rises. Due to the repeated charge and discharge, gate voltage VC receives sequentially capacity coupling at each ϕ_H rise. After the rise of $\phi_{H,LAST}$, the gate voltage VC decays toward the ground level because the gate voltage VC no longer receive capacity coupling. On the other hand, after closing of corresponding HSW, swinging of the gate voltage jumps to each signal line through the capacity component C_H of the equivalent circuit illustrated in Fig. 5.

Before the timing of $\phi_{H,LAST-4}$, the level of signal line changes by ΔV0 as shown on the VBLAST-4. The level of jumping to signal line due to gate voltage VC decay decreases step by step with shifting from $\phi_{H,Last-3}$, to $\phi_{H,LST-2}$, and $\phi_{H,LST-1}$, ... Voltage drop ΔV1, ... ΔV4 for the final four signal line voltages

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VB_{LAST-3}, ..., VB_{LAST} decreases in the order from LAST-3 to LAST.

The ΔV is illustrated schematically in Fig. 7. ΔV of the final four signal lines is smaller than that of all previous signal lines. The decrement increases as the signal line approaches to the final signal line. Accordingly, the band defect is resulted on the final four lines.

As described hereinbefore, according to the present invention, dummy data lines are provided outside the display region in addition to real data lines provided in the display region. The real data lines are scanned horizontally with a sampling timing overlapping on a plurality of data lines, and then additionally the dummy data lines are scanned horizontally with the same sampling timing as scanned on the real data lines, thereby the band defect is eliminated and image quality is improved. Especially, this invention is effective for large size active matrix display devices which utilize increased number of picture elements with dot sequence drive.

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What Is Claimed Is:

1. An active matrix display device comprising:

a plurality of gate lines provided on horizontal lines,

a plurality of data lines provided vertically,

a plurality of picture elements provided at each intersection of said gate lines and data lines which constitute the display region,

a vertical scanning circuit for scanning vertically each gate line sequentially to select picture elements for each horizontal line, and

a horizontal scanning circuit to sample image signals and subsequently write the image signals on picture elements on a selected horizontal line by dot sequential scanning, wherein

said data lines are defined to two sections of real data lines provided in said display region and dummy data lines provided outside said display region which dummy data line intersect with the end section of the gate lines, and

said horizontal canning circuit operates the first scanning horizontally on said real data lines

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with a sampling timing overlapping a plurality of real data lines, and, subsequently to said first scanning, operates the second scanning horizontally also on said dummy data lines with the overlapped sampling timing.

2. An active matrix display device as claimed in claim 1, wherein at least so many said dummy data lines as horizontally scanned simultaneously with a certain overlapped sampling timing are provided.

3. An active matrix display device as claimed in claim 1, wherein dummy picture elements corresponding to said dummy data lines are provided.

4. An active matrix display device as claimed in claim 1, wherein picture elements are provided on only said data lines.

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ACTIVE MATRIX DISPLAY DEVICE

Abstract of the Disclosure

The active matrix display device has a plurality of gate lines, and a plurality of picture elements provided at each intersection of both lines. The data lines are defined to two sections of real data lines Y1, Y2,...., YL provided in the display region and dummy data lines YD1, YD2, YD3, and YD4 provided outside the display region which dummy data lines intersect with the end section of the data lines. The horizontal scanning circuit scans horizontally on the real data lines, subsequently continue to scan on the dummy data lines YD1, YD2, YD3 and YD4 with the overlapped sampling timing. Thereby band defect on the side end of the screen when an active matrix display device is driven dot sequentially is eliminated.

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FIG. 1

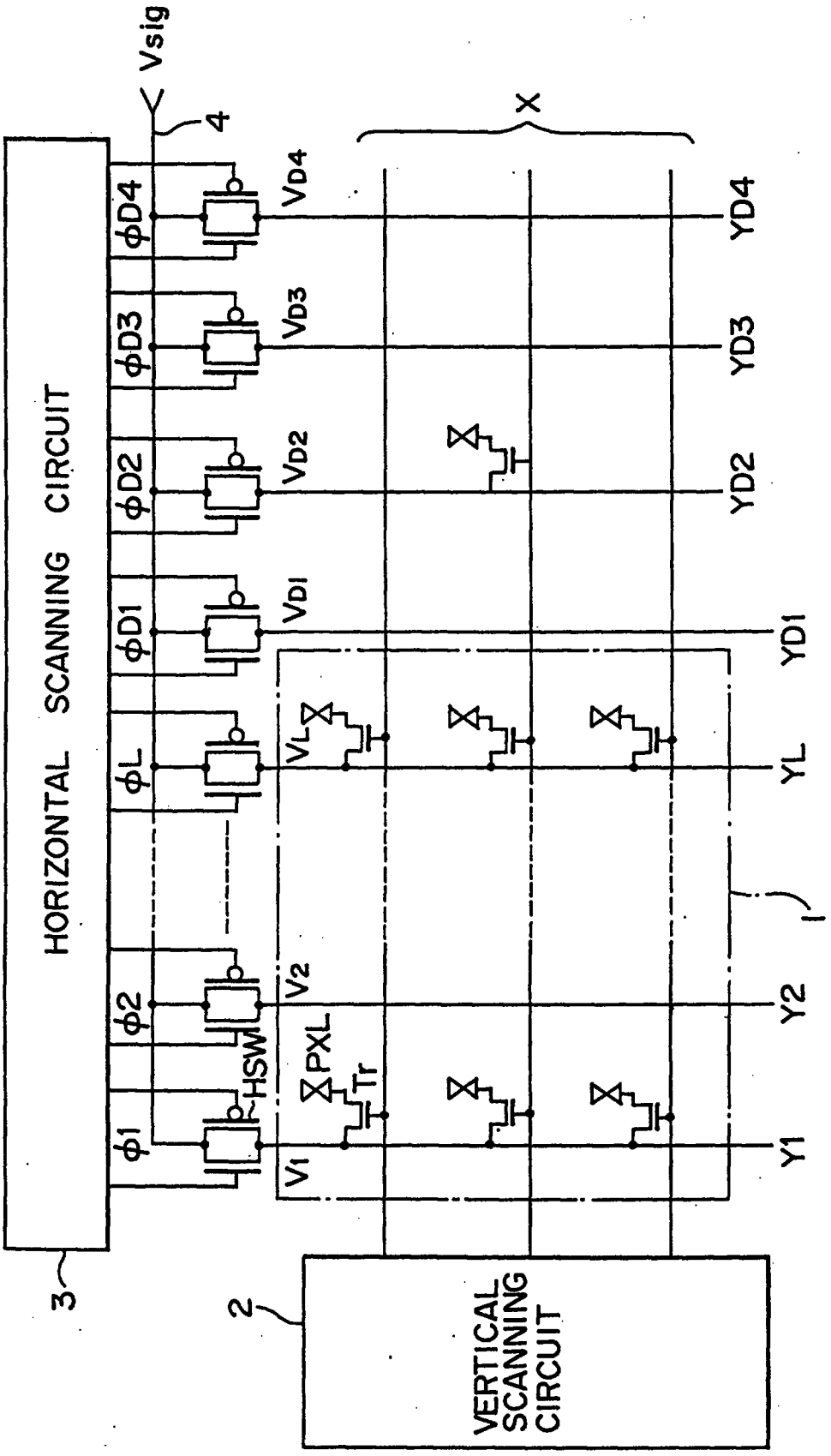

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FIG. 2

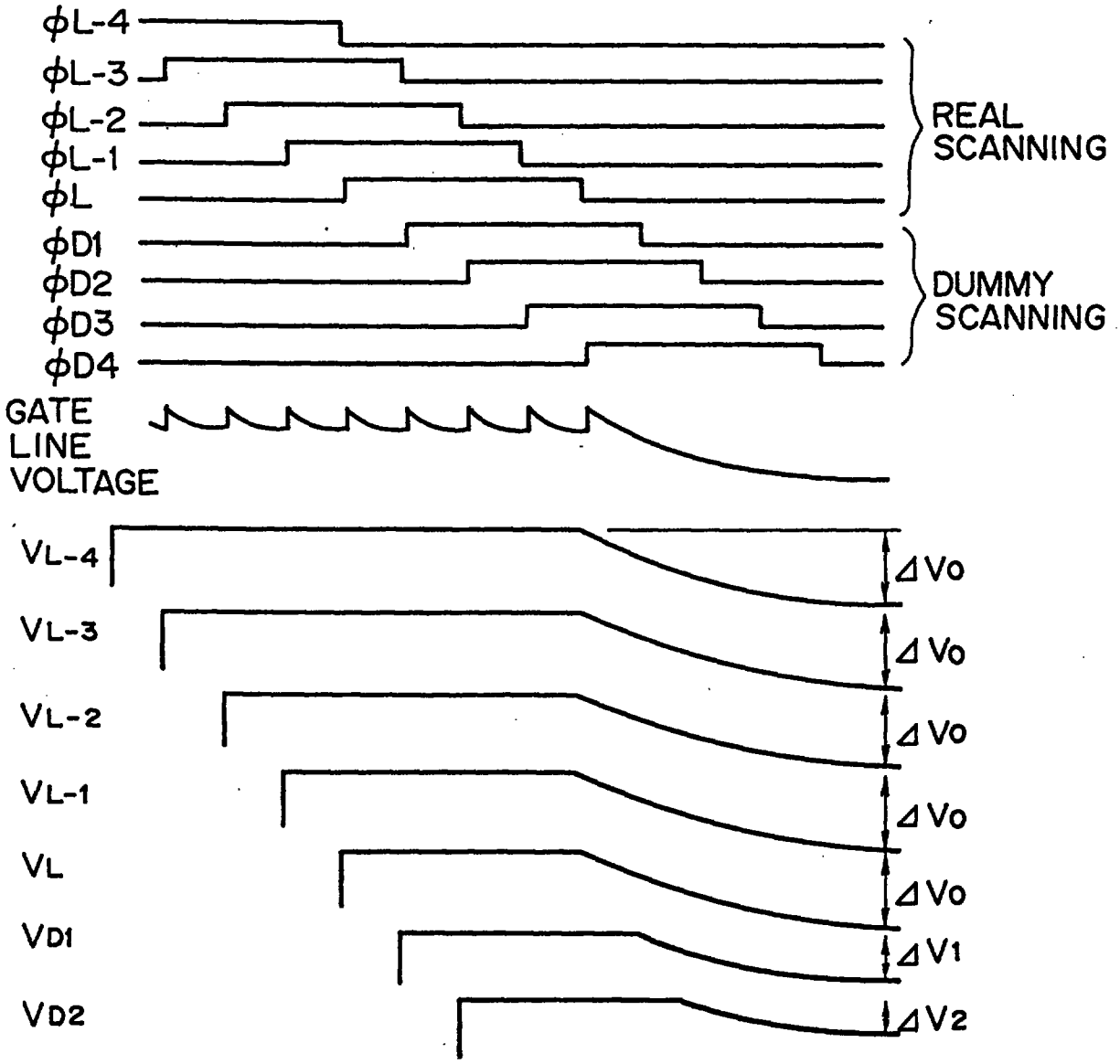

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FIG. 3

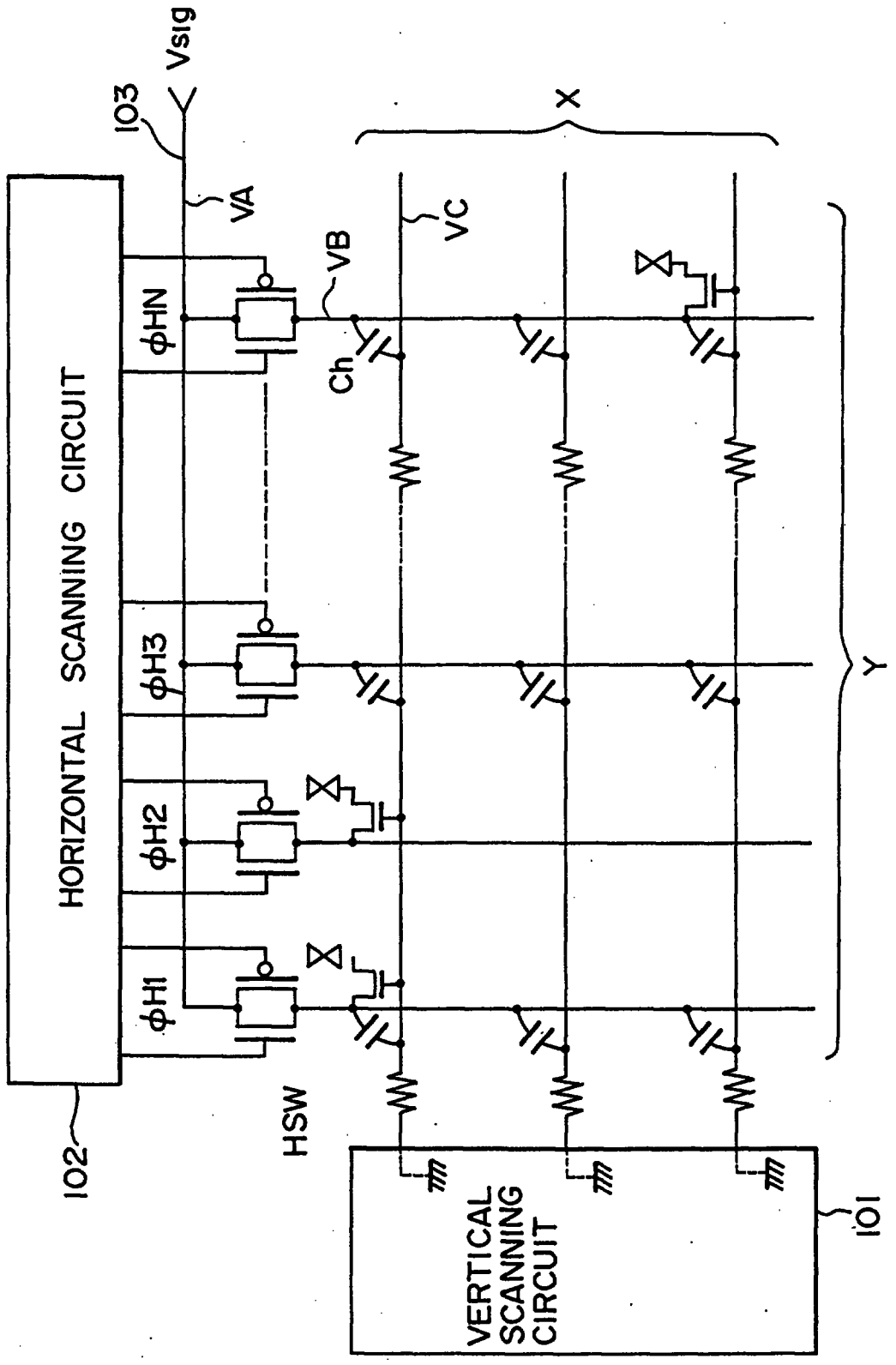

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FIG. 4

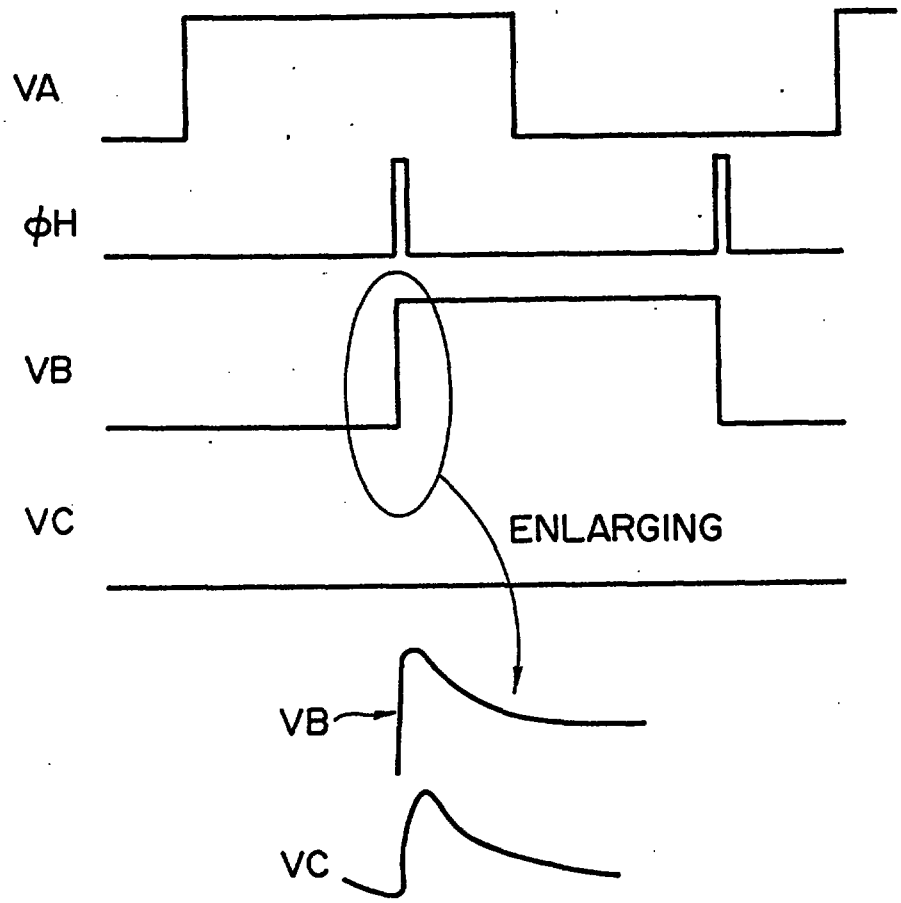

FIG. 5

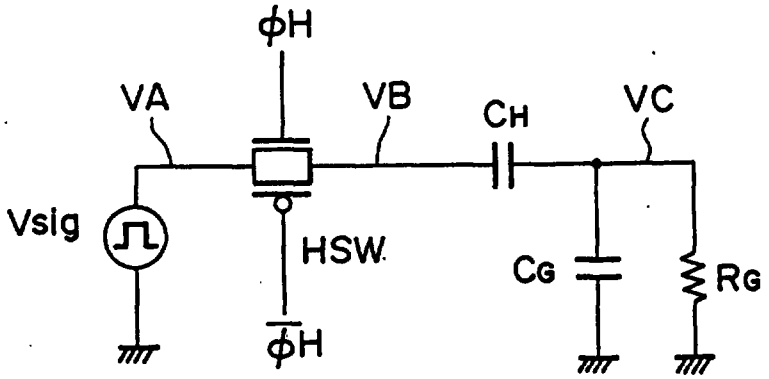

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FIG. 6

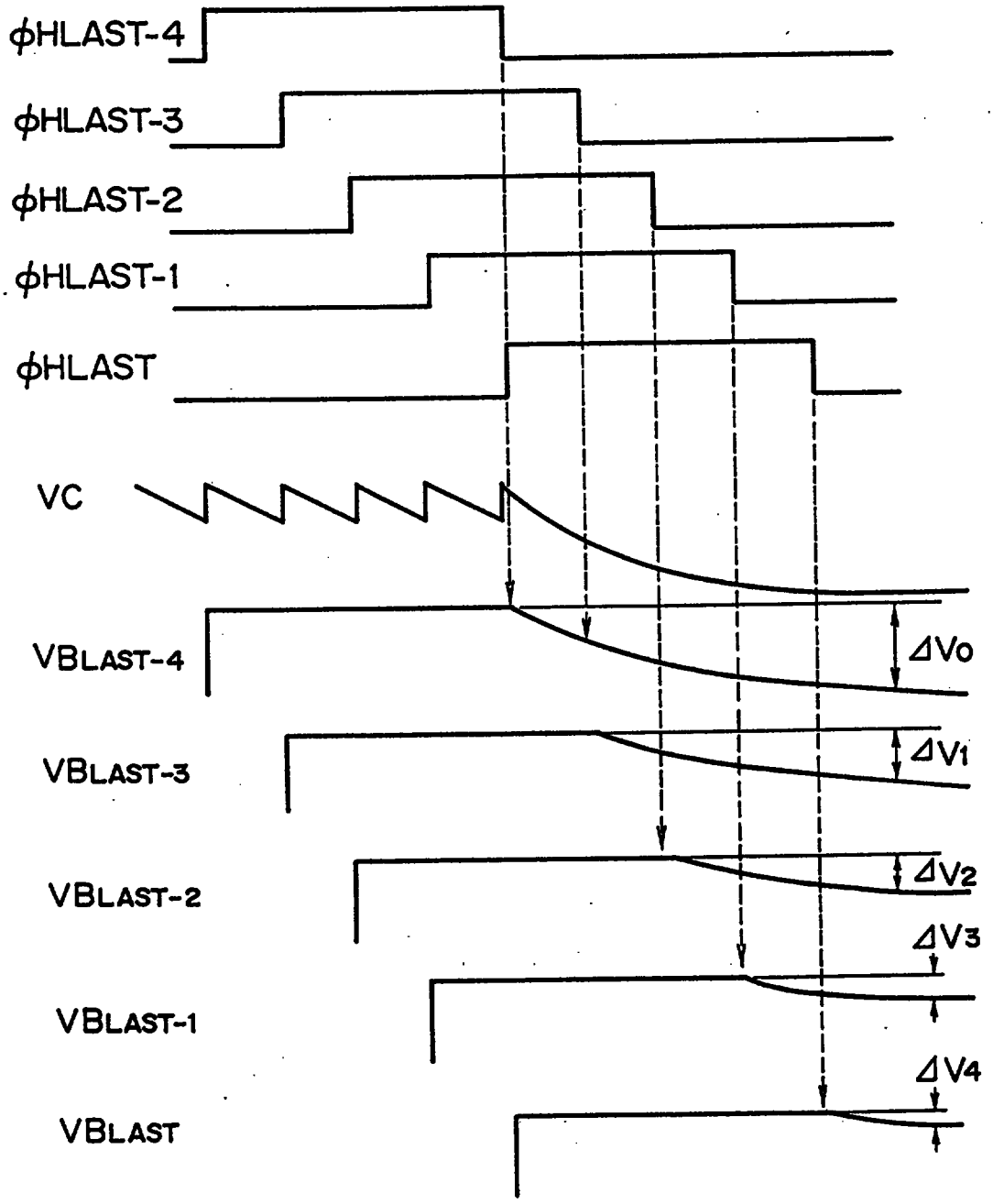

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FIG. 7

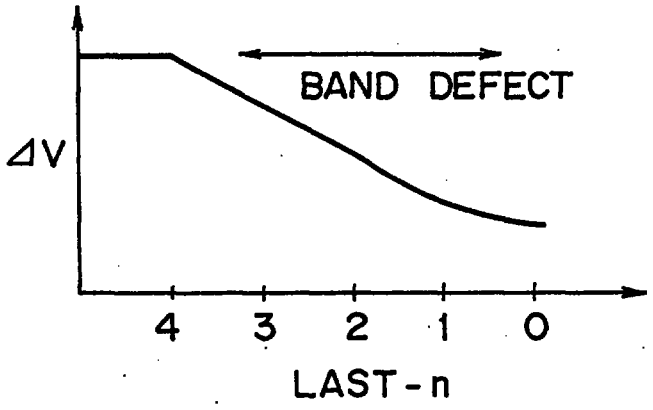

FIG. 8

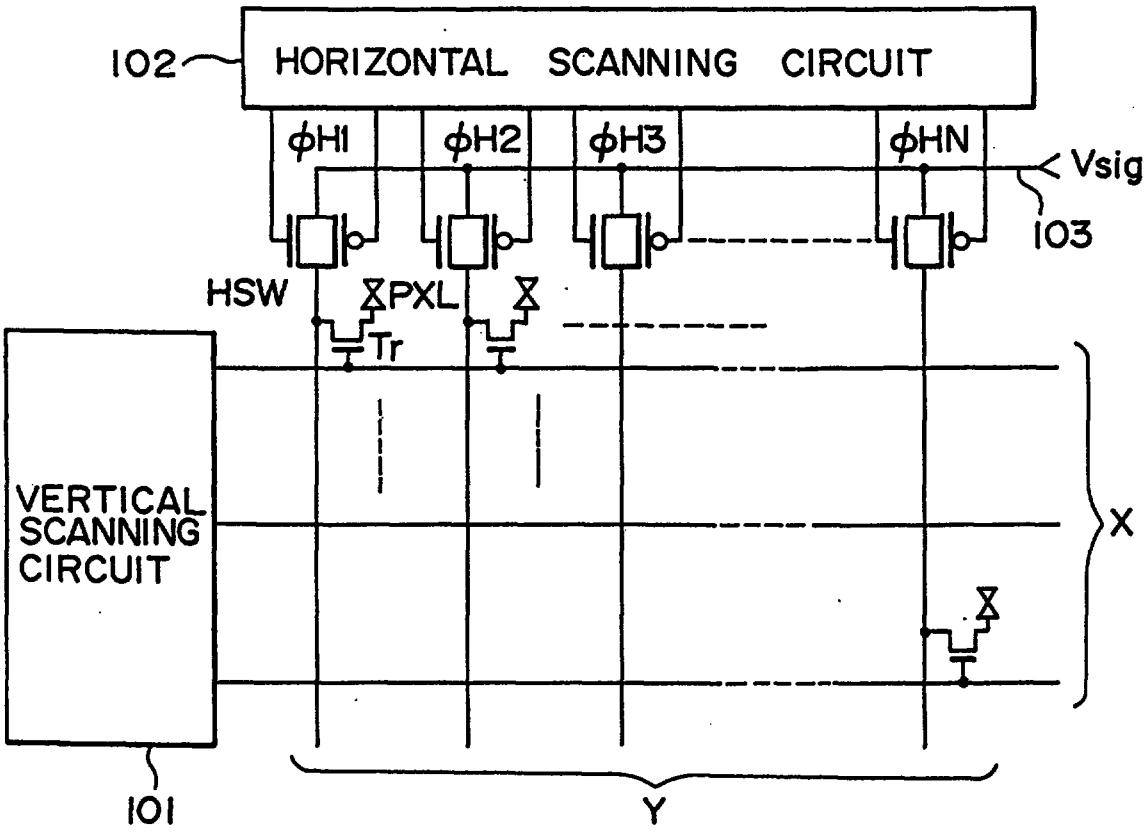

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FIG. 9

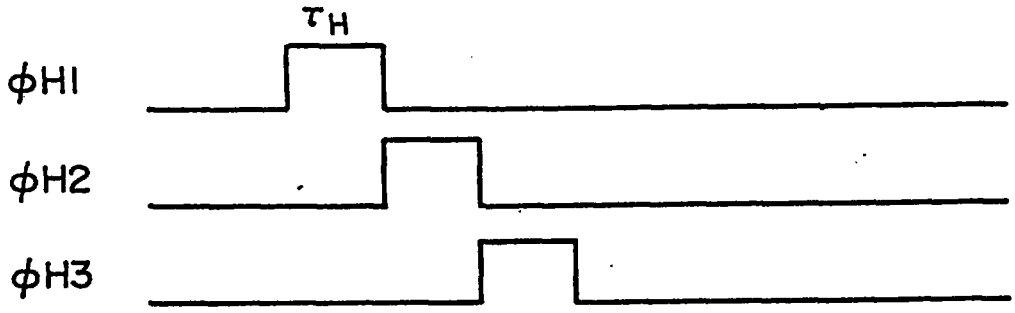


FIG. 10

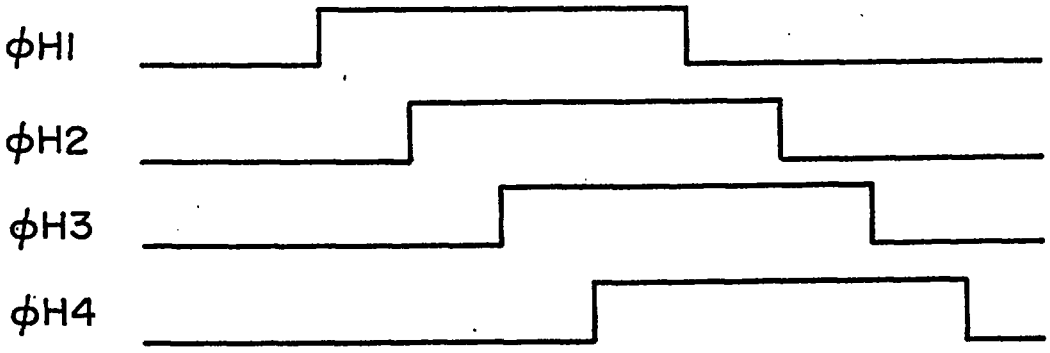
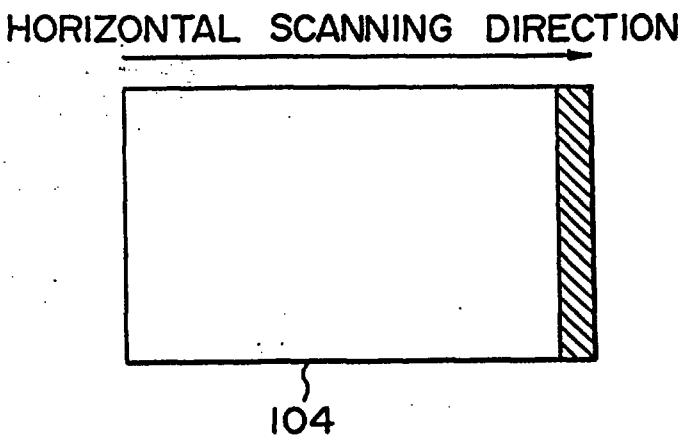


FIG. 11



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ACTIVE MATRIX DISPLAY DEVICE

The active matrix display device has a plurality of gate lines, and a plurality of picture elements provided at each intersection of both lines. The data lines are defined to two sections of real data lines Y1, Y2,...,YL provided in the display region and dummy data lines YD1, YD2, YD3, and YD4 provided outside the display region which dummy data lines intersect with the end section of the data lines. The horizontal scanning circuit scans horizontally on the real data lines, subsequently continue to scan on the dummy data lines YD1, YD2, YD3 and YD4 with the overlapped sampling timing. Thereby band defect on the side end of the screen when an active matrix display device is driven dot sequentially is eliminated.

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What Is Claimed Is:

1. An active matrix display device comprising:

a plurality of gate lines provided on horizontal lines,

a plurality of data lines provided vertically,

a plurality of picture elements provided at each intersection of said gate lines and data lines which constitute the display region,

a vertical scanning circuit for scanning vertically each gate line sequentially to select picture elements for each horizontal line, and

a horizontal scanning circuit to sample image signals and subsequently write the image signals on picture elements on a selected horizontal line by dot sequential scanning, wherein

said data lines are defined to two sections of real data lines provided in said display region and dummy data lines adjacent to an end of the real data lines in horizontal scanning direction on the display region and

said horizontal scanning circuit operates the first scanning horizontally on said real data lines

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with a sampling timing overlapping a plurality of real data lines, and, subsequently to said first scanning, operates the second scanning horizontally also on said dummy data lines with the overlapping sampling timing.

2. An active matrix display device as claimed in Claim 1, wherein said dummy data lines are provided at least as many as the number of horizontally scanned simultaneously with an overlapping sampling timing.

3. An active matrix display device as claimed in claim 1, wherein dummy picture elements corresponding to said dummy data lines are provided.

4. An active matrix display device as claimed in claim 1, wherein picture elements are provided on only said data lines.